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MULTI-SYSTEM LASER SAFETY SHUTTER CONTROLLER

E. Thomas Kensky
Electromagnetic Materials & Survivability Divison

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WRIGHT RESEARCH AND DEVELOPMENT CENTER
AIR FORCE SYSTEMS COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OHIO 45433-6533

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E. Thomas Kensky

E. THOMAS KENSKY
Electronic & Optical Materials Branch

Robert L Denison

ROBERT L. DENISON, Chief
Electronic and Optical Materials Branch
Electromagnetic Mat'ls & Surv. Division

FOR THE COMMANDER

William R Woody

WILLIAM R. WOODY, Chief
Electromagnetic Mat'ls & Surv. Division
Materials Laboratory

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The use of lasers in research laboratories has become commonplace. With this increased use of lasers comes the inherent danger from laser radiation to the user. While burns are thought of as the primary danger from lasers, a more immediate hazard is the loss of eye sight. This danger increases in laboratory environments where it is impractical to completely enclose the beam path. To provide an increased level of safety for these instances, a laser safety shutter controller has been designed and implemented. This system provides an effective interface between the laboratory entrances and accompanying safety shutters to provide laser beam blockage during a laboratory breach. In addition, this system provides a host of convenience features that allow the laser user to easily control laser emission. These features include shutter and interlock control of up to eight independent lasers, push button shutter control and infrared remote control.

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1.0 INTRODUCTION

In the modern laboratory environment, the laser has become commonplace. From materials research and testing to communications and optical computing, lasers have proven to be valuable tools for research. Along with this usefulness, lasers pose an inherent safety hazard. One immediately thinks of burns as the primary hazard of laser operation; however, this is not the case. A more important concern is the ability of laser light to blind an unsuspecting individual. Surprisingly low intensity levels of laser radiation can cause permanent vision loss before the human eye can react. For this reason, vision safety should be of paramount importance in a laser environment.

The foremost method of vision protection from laser radiation is the use of safety goggles. Goggles with filters for blocking laser light at various wavelengths are available from a multitude of manufacturers. If chosen and worn properly, they provide adequate protection to those working with lasers while still allowing adequate visual perception to perform normal laboratory functions.

While safety goggles provide protection to announced visitors or those individuals who regularly work with lasers, the unexpected guest is still at extreme risk. To provide protection to these individuals, most lasers incorporate an interlock mechanism that shuts the laser down during an unexpected breach of the laser work area. Usually a switch of some sort is connected to the entrance doors of the laboratory that activates the interlock. However, while this type of mechanism is extremely useful in a secure laboratory, it may not be well suited for a more "heavily travelled" lab. This is because most interlock mechanisms operate by shutting down the laser power supply. Doing this requires that the laser be restarted after each shutdown. This situation is very inconvenient and may be damaging to the laser. An alternative to this system is a safety shutter.

A safety shutter functions by blocking the laser beam when a laboratory intrusion occurs. This is more convenient than the interlock mechanism, and it produces no strain on the laser system. The safety shutter can be controlled the same as an interlock, and it provides a convenient means of stopping the laser beam when the rearrangement of an experiment is required. The following documentation describes the design and implementation of such a shutter system.

1.1 SHUTTER CONTROLLER SYSTEM REQUIREMENTS

Safety is of paramount importance when designing a shutter control system for a research environment employing lasers. However, convenience and ease of use are also factors that should be considered. Within this scope, a safety shutter system should provide fail-safe protection while still allowing the user easy access to the laser beam. Meeting these conditions will provide the user with maximum benefits and minimum inconvenience.

For fail-safe operation, the shutter system must ensure three conditions. First, the laser must not be allowed to operate when the safety shutter system is turned off. This will prevent the inadvertent use of the laser without safety protection. Second, if the shutter system fails to operate properly, then all laser systems in the laboratory must be turned off. This provides maximum protection in the event of power failure to the system or improper operation of the actual shutters. Lastly and most important, the shutter system must provide for laser beam blocking whenever a breach of the laboratory occurs. The system must close all shutters whenever an entrance to the laser area is opened regardless of whether the opening was planned or not.

To be convenient to the user, the system must allow the laser beam to be blocked and unblocked at will in a number of ways all of which are easily accessible to the laser user. This could include the use of manual switches placed in strategic

locations around the laser, remote control mechanisms or even computer control. In addition, the shutter system should be easily expandable to allow the addition of more laser systems within the laboratory.

Another desirable feature of a safety shutter control system is an open-ended output. The shutter control system should be flexible enough to allow control of various types of shutters. For low power lasers, this will include various electromagnetic shutters. For higher power lasers, this may include beam dumps and motorized mirrors. A good system design will be general enough at the output stage to allow adaptation to all of these beam control mechanisms.

All of these requirements can best be met with a microprocessor-based controller. This will allow the use of conditional decision-making to distinguish between emergency and convenience situations. In addition, a microprocessor based system will allow flexibility in the type and number of user-executable functions for shutter control that cannot be obtained any other way.

1.2 SYSTEM OVERVIEW

The shutter controller is designed around the Motorola MC6802 8-bit microprocessor. The system has 2048 bytes of erasable programmable read-only memory (EPROM) for system program and operating instructions and 128 bytes of random access memory (RAM) internal to the MC6802 for stack operations and temporary storage. The shutter controller operates in a two data bus configuration with one bus serving the microprocessor and the other bus acting as a gateway for data from peripheral devices.

For communication to external safety devices, the system uses three 8-bit output ports and an 8-bit input port. Two of the output ports serve as drivers for safety shutters and interlocks, and the third port drives indicator lights to convey the status of

the safety shutters to the user. The input port accepts input data from an external driver that indicates the actual state of the shutters so comparison can be made to the expected state. The data from this input port are used primarily to determine if a shutter closure failure occurred.

User interface to the shutter controller system is accomplished through the use of interface cards. These cards, called slot cards, perform the dual function of signalling the system that an action is to be taken and indicating the specific nature of the requested action. The cards allow the user to control the shutters and/or interlocks of each laser connected to the system via the use of switches, remote controls and computer interfaces. It is through the use of the second data bus that these cards communicate with the microprocessor.

The controller operates through an interrupting scheme. All actions to be taken by the controller are initiated by an interrupt of some sort. In the case of a laboratory breach, the interrupt service has highest priority and is nonmaskable. In other words, the system has no means of ignoring a breach interrupt. This provides maximum protection in case of emergency. This type of interrupt will take precedence over all other activities of the system with the exception of a hardware reset.

The other type of interrupt received by the controller is from the interface cards. This interrupt operates on a pseudo-priority basis and is maskable. For this case, any interface card can signal the system for service, but the signal can be ignored when an emergency interrupt (i.e. nonmaskable) arises.

The service scheme for the slot cards is somewhat unique. Any card in any slot of the system can cause an interrupt, but once recognized, the system will temporarily ignore all others. The system then searches the slots in ascending order to determine which card sent the interrupt. Once the interrupting card has been found and serviced, the interrupt is cleared and any other outstanding interrupts can be serviced.

If two cards send interrupt requests simultaneously, the card with the lowest slot address will be serviced first.

The shutter control system has been designed to handle up to eight laser shutters and interlocks. In addition, the slot cards have been designed to allow control of any shutter or interlock by simply changing its command code. This design gives maximum flexibility to the user for customizing to a particular need and also allows for change when the user's needs change.

1.3 SHUTTER CONTROLLER ALGORITHM SPECIFICS

When in operation, the shutter controller performs a set of very specific tasks. These tasks form the operation algorithm and are separated into three types. The first task performs initialization to the system. The other two tasks service interrupts. The first answers laboratory breach requests, and the other answers user convenience requests.

The initialization task is initiated in one of three ways. It occurs during power-up, upon hardware reset or upon receiving a reset command from a slot card. In all cases, during initialization the controller performs the following set of tasks. The system first disables any convenience requests, then closes all shutters and interlocks and finally updates the shutter indicator lights. The result is to enable all lasers and block all beams. The controller then resets all slot cards and enables convenience interrupts. Upon completion of these tasks, the controller enters a wait state.

When the controller receives an interrupt indicating that the laboratory was breached the first action to be performed, after disabling convenience interrupts, is to close all shutters on all lasers. The controller then enters a delay routine to allow the shutters sufficient time to close and settle. The state of these shutters is then read, and if they were all found to be closed, the controller begins a polling routine of the entrance

to the laboratory where the breach occurred. If the controller determined that the shutters did not all close (i.e. a malfunction) it immediately opens all interlocks and subsequently turns off all lasers. It should be noted that even under these circumstances, the breached laboratory entrance is monitored. No further action can be taken to affect either shutters or interlocks until the breach to the laboratory is secured. Once it has been secured, the controller returns to a wait state.

The third type of task performed by the controller is servicing user convenience interrupts. These are sent by the slot cards and are primarily used to open or close shutters and interlocks for the convenience of the laser operator. The operations performed in this routine are more involved than those of the previous routines. After postponing further convenience interrupts, the controller polls the slot cards to determine which one is requesting service. Once this has been determined, the controller reads an 8-bit command byte from the interrupting slot card. This byte is put through a series of tests to determine if it is valid, and if so then the appropriate action is taken. If the byte was invalid, the slot card is reset and the controller returns to a wait state. It should be noted that the convenience service routine will be aborted during execution if a lab breach interrupt is received.

The specific action to be taken by the controller is dictated by the code sent by the slot card. This code can cause any one of 37 actions to be taken. Five of these actions are global in nature in that they affect more than one shutter or interlock at a time. The most global command is the reset command. This command causes a total reset of the system. The other four global commands either open all shutters or interlocks (two separate codes) or close all shutters or interlocks (two separate codes).

The remaining 32 codes that can be sent by a slot card are used to open or close individual shutters or interlocks. The controller acts upon these codes by interpreting them as offset addresses to an action table contained in the EPROM. The controller uses this offset address to obtain a byte of information from the action table.

This is then used in conjunction with the present state of the shutters or interlocks to effect the appropriate change.

The hardware design in conjunction with the operating algorithm provides for an effective shutter control system. Both safety and convenience issues of users dealing with exposed-beam laser systems is addressed. In addition, a great deal of flexibility is inherent to the system providing open-ended control and expandability to meet present and future needs of laser laboratories.

2.0 SYSTEM DESCRIPTION

The laser shutter controller's hardware is separated into two catagories. The first is the microprocessor and its associated support circuitry. The second is the slot cards. The structure and function of the circuitry for each of these will be discussed in separate sections.

2.1 THE MICROPROCESSOR

A block diagram of the microprocessor circuitry is shown in figure 1. The heart of the controller is the Motorola MC6802 8-bit microprocessor. This processor features an 8-bit data bus and a 16-bit address allowing access to a full 64 kilobytes of contiguous memory. The processor supports the full MC6800 instruction set and has 128 bytes of on-board RAM. Other features include an on-board clock for system timing and two separate hardware interrupt lines.

The MC6802 has a contiguous memory map. This means that all devices in a system designed around the MC6802 have separate addresses and are treated as memory locations. This facilitates system design by allowing the use of the address lines and the read/write control lines for all device decoding. This scheme, however, also requires mutually exclusive address decoding for each device including both memory addresses and I/O ports.

As configured in the laser shutter controller, the MC6802 has three input control lines that directly affect system operation. The first is the reset pin. Driving this control line low will immediately cause the microprocessor to internally initialize and then execute the initialization program to reset the rest of the system. Reset is executed automatically on power-up and can be initiated manually when required. The second and third control lines are the external interrupts. The first is the nonmaskable interrupt (NMI), and it is initiated by breaches to the laboratory environment. The second is a maskable interrupt (IRQ), and it is initiated by the slot cards whenever service is required.

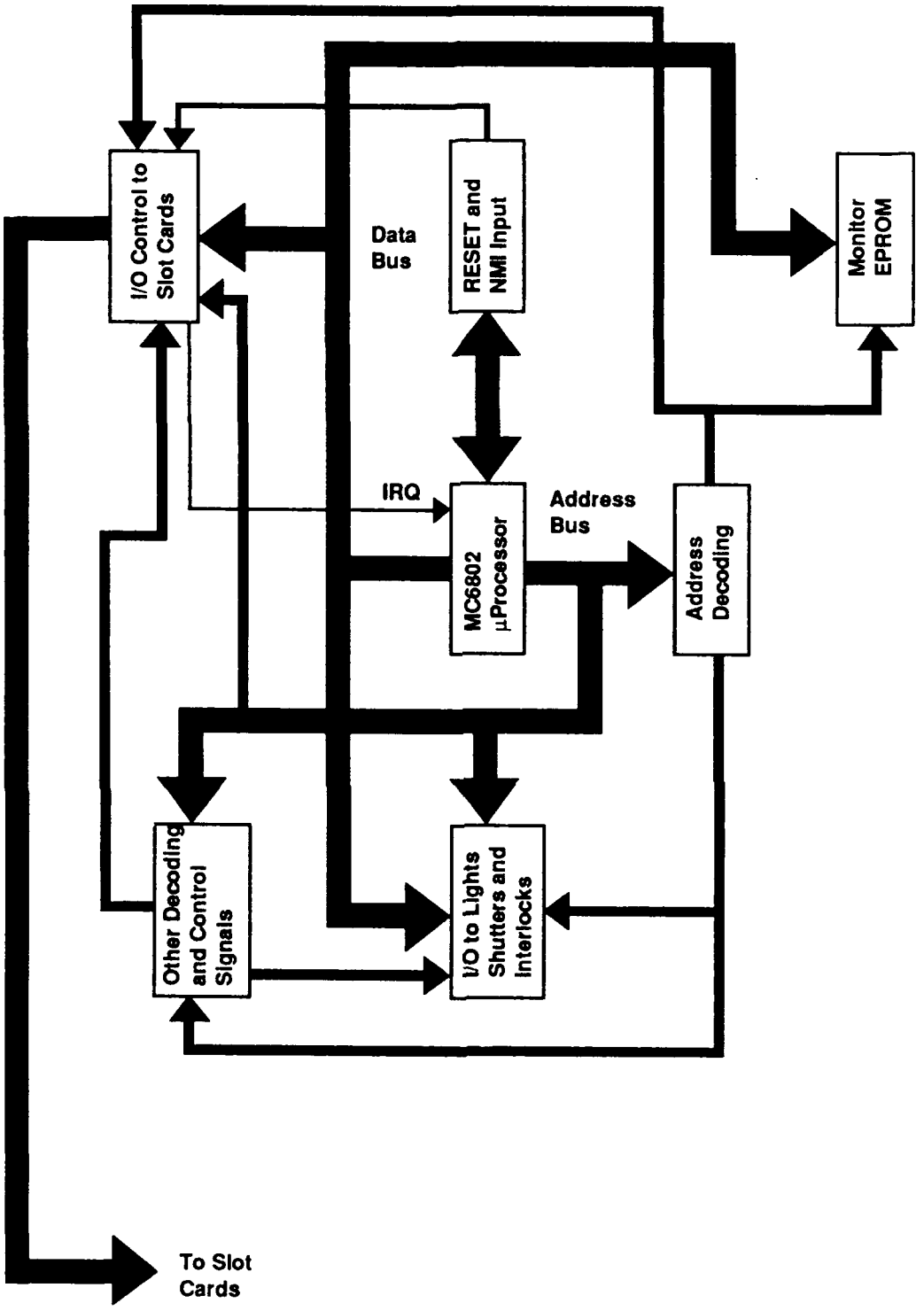


FIGURE 1 - System Block Diagram

Within the MC6802, the Reset and the NMI are considered nonmaskable service requests. What this means is that the microprocessor cannot ignore them. An occurrence of either of these requests will always cause the microprocessor to search for, and execute a service routine. The IRQ, however, is considered as a maskable interrupt. The MC6802 can ignore IRQ interrupts if internal conditions are properly set.

One very useful feature of the MC6802 is its internal clock circuitry. The microprocessor requires only the addition of an external crystal and two netting capacitors for clock operation. This feature helps reduce the component count when designing a system. In addition, the microprocessor can be driven externally using a crystal clock module which can further reduce the component count.

The speed of the MC6802, called the cycle time, is a function of the clock frequency. The limits of the clock frequency can be found in the data sheets for the MC6802, and the relationship between the clock frequency and the cycle time is given in equation 1.

$$\text{Cycle Time} = \frac{4}{\text{Clock Frequency in Hz}} \text{ Seconds} \qquad (1)$$

A typical clock frequency is 3.579545 MHz (T.V. color burst crystal) yielding a cycle time of 1.118 μS.

Instruction execution within the MC6802 generally requires several cycle times. The number of cycles required to execute an instruction varies and is directly related to the instruction itself. Typically, the number varies between two and eight cycles depending on the operations involved in the instruction and the addressing. The number of cycles for each instruction is usually included in the data sheets for the MC6802.

2.2 THE SYSTEM BUS STRUCTURE

The laser shutter controller has a three bus architecture. The microprocessor communicates to all devices using the address bus (including the timing control signals) and two data buses. The address bus is 16 bits wide providing 64 kilobytes of addressing capability, and the two data buses are 8 bits wide allowing single-byte operation. The address bus and one of the data buses are interfaced directly to the MC6802 microprocessor and are used for addressing, communication and data transfer between devices. The second data bus is buffered from the first data bus and is used for data transfer to the slot cards.

2.2.1 THE ADDRESS BUS DECODING SCHEME

As mentioned previously, the address decoding scheme employed in the laser shutter controller provides for a contiguous 64-kilobyte memory map in which all devices are assigned one or more addresses. Each address, whether pointing to a real memory location or to an I/O port, is mutually exclusive. This scheme prevents inadvertent access to a device but neccessarily increases the amount of address decoding logic.

The memory map for the laser shutter controller is shown in figure 2. The memory map can be thought of as having three distinct sections. The first section is the nonvolatile memory (EPROM) where the controller's operating system resides. The second section is the read/write memory (MC6802 internal RAM) where temporary data are stored and where stack operations occur. The third section of the memory map is the I/O section. This includes all I/O to the lasers and shutters as well as the slot cards and the hardware reset signals.

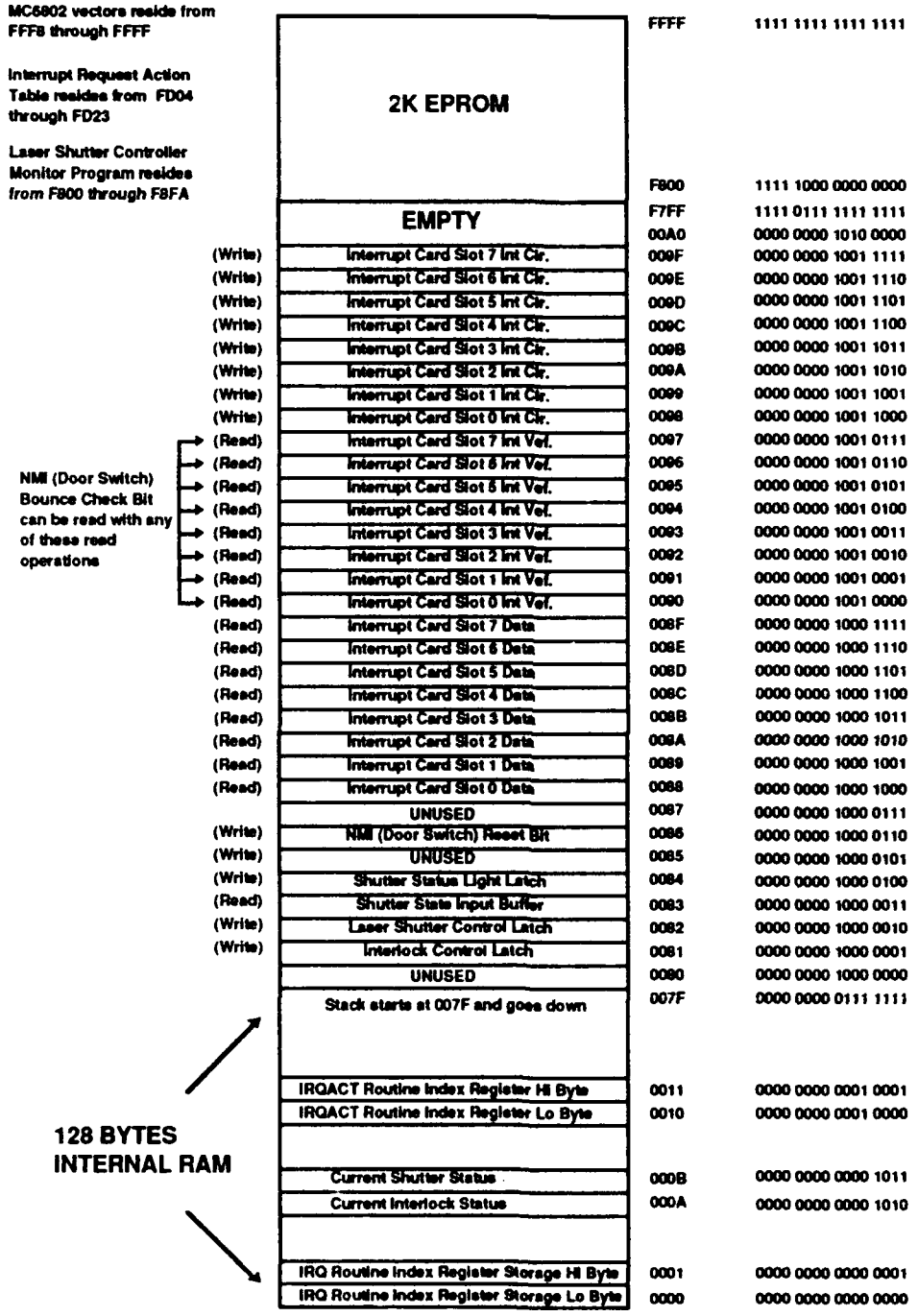


FIGURE 2 - Laser Shutter Controller Memory Map

Due to the nature of the MC6802 microprocessor, the location for each section in the memory map is not very flexible. Since the RAM for the microprocessor is internal, its location is fixed. The 128 bytes of RAM for the microprocessor is located from $0000 to $007F (hexadecimal addresses). The MC6802 also requires that the system vectors be located in the highest-most address space in the map. The MC6802 has a total of four double-byte system vectors and they are required to be in the locations $FFF8 through $FFFF (see table 1). Since the microprocessor must access these vectors to perform vital operations, they are kept in non-volatile memory. This strongly suggests placing the operating system software in the same non-volatile memory. If this is done, then the operating system software resides in the highest memory locations. For the laser shutter controller, there are 2 kilobytes of EPROM, and it resides from $F800 through $FFFF. Both the system vectors and operating system software is placed in this EPROM.

The third section in the memory map has the greatest flexibility in location. This section contains all of the I/O ports, the slot card addresses and the system reset control signals. The choice of location in the map for these device addresses is made solely on the basis of hardware implementation. The goal is to minimize the hardware required to exclusively decode for these locations. Placing all of the I/O addresses in a contiguous block in the memory map allows the use of a single IC address decoder and a few supporting logic gates to decode for all addresses. The whole block is placed as low as possible in the map as a convenience (refer to figure 2).

In addition to the address lines, the MC6802 uses three control signals when sending out a valid address. These three signals are the VMA signal, the R/$\overline{W}$, and the E clock. These signals are logic level active (i.e., not transition sensitive) and must be used when addressing devices on the processor's bus. The VMA signal is an active logic high signal when valid and indicates that there is a valid address on the MC6802's address bus. The R/$\overline{W}$ signal is a two-state

TABLE 1 - MC6802 System Vectors

VECTOR		DESCRIPTION
MSB	LSB	
$FFFE	$FFFF	RESET
$FFFC	$FFFD	NON-MASKABLE INTERRUPT (NMI)
$FFFA	$FFFB	SOFTWARE INTERRUPT
$FFF8	$FFF9	INTERRUPT REQUEST (IRQ)

signal, and it distinguishes between a read operation and a write operation. If the microprocessor is performing a read operation, this signal will be high. If the operation is a write operation, the R/$\overline{W}$ signal will be low. The last signal is the E clock and it provides the synchronization for each microprocessor operation.

Actually accessing the contents of an I/O port or a memory location is accomplished by performing logical operations on the states of the address bus and the MC6802's control signals to produce a unique decoding signal. This decoding signal, in conjunction with the address from the microprocessor, is used to activate a device on the bus.

For the laser shutter controller, all decoding signals are active low and logic level active (as opposed to edge-triggered). The address decoding scheme for each type of device is explained in detail in the following paragraphs. A complete set of schematics for this system can be found in section 5.

2.2.1.1 EPROM DECODING

The decoding circuitry for the EPROM is shown in figure 3. The EPROM is an industry standard 2716. The 2716 has 2K X 8 bytes (K=1024) of nonvolatile storage capacity and is erasable using ultraviolet light. In addition to the address lines, there are two control lines that

can be used to select the 2716. These are the chip enable ($\overline{CE}$)and the output enable ($\overline{OE}$). Both of these signals are active low and in the implementation in figure 3 only one ($\overline{OE}$) is used.

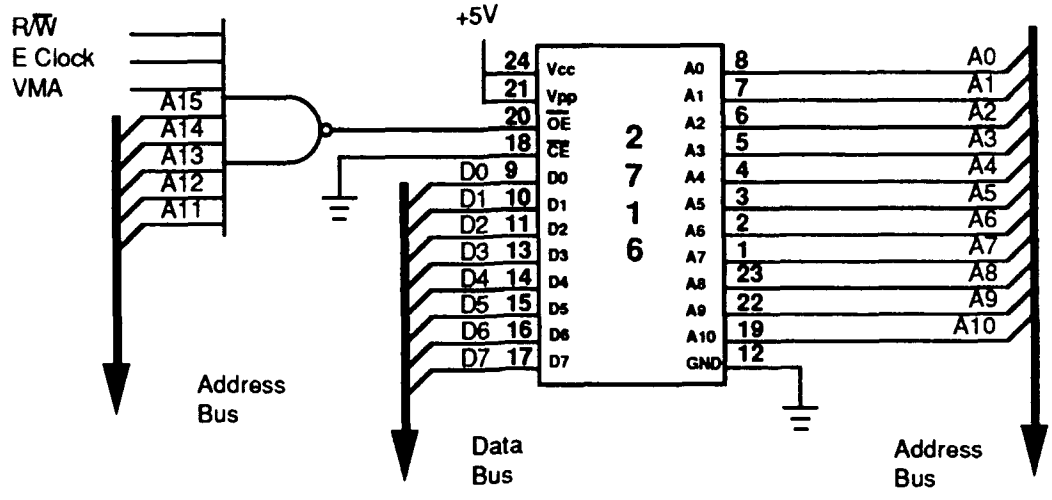


FIGURE 3 - EPROM Decoding

When the $\overline{OE}$ signal is driven low, the data lines of the 2716 come out of the high impedance state and the data or instruction op-code that resides in the EPROM is placed on the data bus. The $\overline{OE}$ signal is produced by performing the logical NAND operation on the address and control lines of the MC6802. This is shown in equation 2.

$$\overline{OE} = \overline{A11 \cdot A12 \cdot A13 \cdot A14 \cdot A15 \cdot VMA \cdot E \cdot R/\overline{W}} \qquad (2)$$

The output enable pin on the 2716 is active low and the data within the 2716 will appear on the bus when this pin is logic low. In order to generate $\overline{OE}$, the address lines A11 through A15, the valid memory address signal, the E clock and the R/$\overline{W}$ signal must all be logic high. With A11 - A15 being high, the allowable addressing range that will place the EPROM in the active state is $F800 through $FFFF. This corresponds exactly to the EPROM location in the

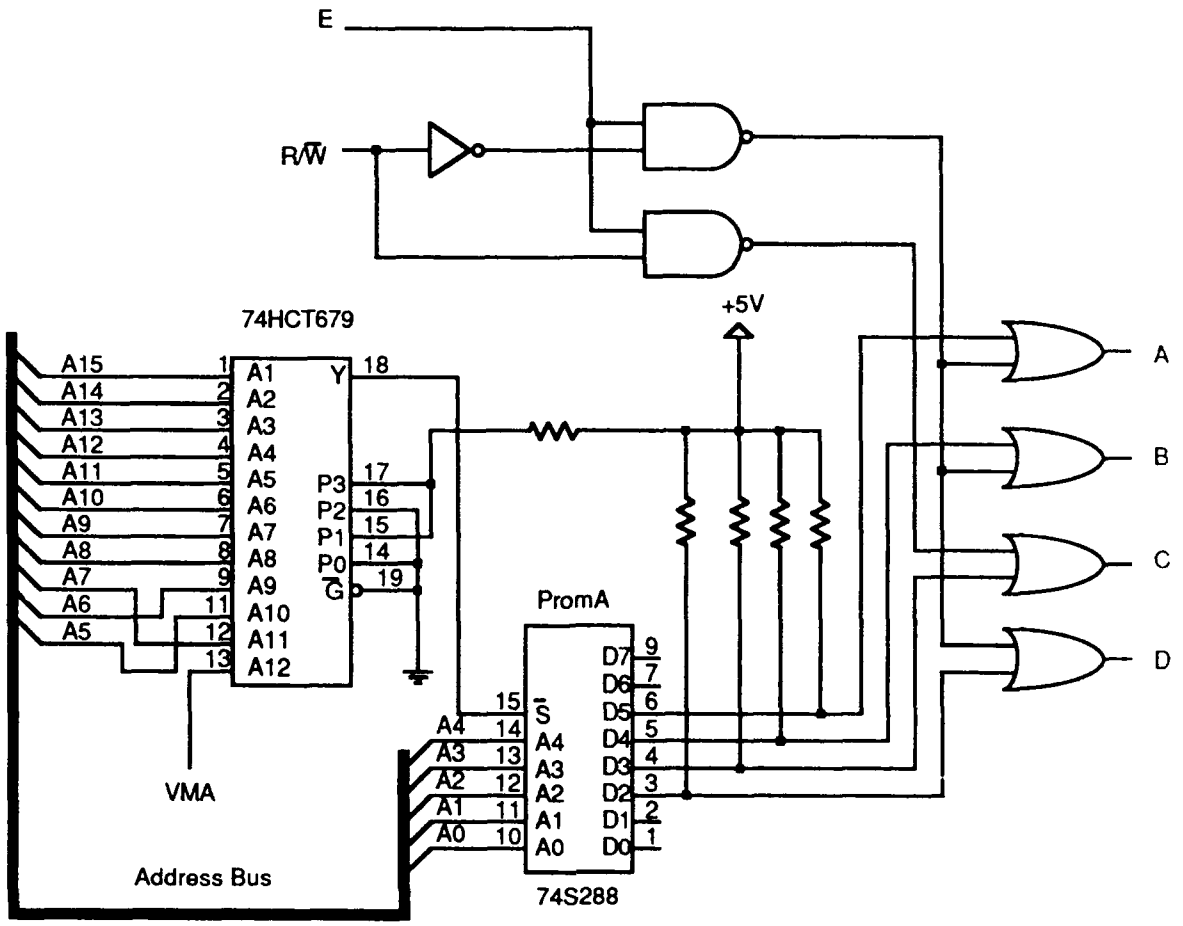
memory map. The other three control signals shown in figure 3 must also be high to accommodate the timing requirements of the microprocessor.

2.2.1.2 I/O PORT DECODING

The address decoding circuit for the I/O ports is shown in figure 4. The control signals generated here enable three 8-bit latches and an 8-bit buffer that interact with the laser systems. Two of the latches affect the laser shutters and interlocks, and the other latch drives the LED display that indicates the current state of the shutters (open or closed). The buffer is an input that is used to test the actual state of the laser shutters.

The decoding scheme used here employs a programmable read only memory device (PROM) that contains a set of bit patterns in each of its memory locations. These bit patterns are used in conjunction with the microprocessor's control signals to enable and/or latch data to the I/O ports. The PROM used is a 74S288 bipolar PROM with 32 bytes of storage. The address lines of this PROM are driven by the lowest 5 address lines of the system (A0 - A4), and this places all of the data in the PROM, and thus the control signals they represent, in sequential order.

According to the system memory map (figure 2), the I/O ports are in locations $0081 through $0084. In order to decode the control signals in the PROM for these locations, the base address of $0080 is decoded and used as the enable signal for the PROM. This decoding is performed by a 12-bit address comparator (74HCT679) that is driven by the higher order address lines of the system. The comparator's address inputs are connected to A5 through A15 of the system address bus and the VMA signal. The decoder is programmed through the use of its control lines (P0-P3) to check for all logic lows on address lines A5, A6 and A8 through A15, and for logic highs on A7 and the VMA line. This occurs when the base address is $0080 and the VMA indicates that there is a valid address on the bus. When this condition occurs, the 74HCT679 places a low at its output and enables the output of the PROM. The address on the



A - Interlock Latch Control Signal
B - Shutter Latch Control Signal
C - Shutter State Buffer Read Enable Signal
D - Shutter State Output Lights Latch Control Signal

FIGURE 4 - I/O Port Decoding

lowest address lines connected to the PROM then determine which particular bit pattern will be output from the PROM. The logic equation for the output of the 74HCT679 is given in equation 3.

$$\overline{Y} = (A7 \cdot VMA) \cdot \overline{(A5+A6+A8+A9+A10+A11+A12+A13+A14+A15)} \qquad (3)$$

When used in this fashion, the PROM serves as one quarter of a 5-line-to-32-line decoder/demultiplexer. As can be seen in table 2, the bit patterns in the PROM consist of all logic highs (all 1's) in 7 of the 8 bit locations and a logic low (a 0) in the remaining bit. The 0 appears in a different bit position for each byte in the PROM and when the microprocessor addresses an I/O port the PROM places one of these bytes at its output. The bit in this byte that is low is the only active bit, and it is logical ORed with the microprocessor's control signals to enable one and only one of the I/O port latches/buffer.

With this decoding scheme, only four of the eight data lines are used for enabling the I/O ports. To take advantage of the other four data lines, the I/O ports, the system control signals and the slot card addresses are all placed in a contiguous block within the memory map. This allows two of the remaining four data lines to be used for generation of other control signals for the system. In addition, another identical PROM is connected in parallel to perform a similar decoding function for the slot cards.

The four specific signals that control the I/O ports are the Interlock Latch Control signal, the Shutter Latch Control signal, the Shutter State Buffer Read Enable signal and the Shutter State Output Lights Latch Control signal. These signals are derived by logic ORing the PROM outputs with control signal combinations from the microprocessor. Referring to the designations given for the control signals in figure 4, the logic functions for each control signal can be seen in equations 4 through 7.

$$A = \overline{\overline{E \cdot (R/\overline{W})}} + D5 \qquad (4)$$

$$B = \overline{\overline{E \cdot (R/\overline{W})}} + D4 \qquad (5)$$

$$C = \overline{\overline{E \cdot (R/\overline{W})}} + D3 \qquad (6)$$

$$D = \overline{\overline{E \cdot (R/\overline{W})}} + D2 \qquad (7)$$

TABLE 2 - PROM A Memory Map

Address HEX	A4	A3	A2	A1	A0	Description	Data D7	D6	D5	D4	D3	D2	D1	D0	HEX
00	0	0	0	0	0		1	1	1	1	1	1	1	1	FF
01	0	0	0	0	1	Interlock Latch	1	1	0	1	1	1	1	1	DF
02	0	0	0	1	0	Laser Shutter Latch	1	1	1	0	1	1	1	1	EF
03	0	0	0	1	1	Shutter State Input Buf.	1	1	1	1	0	1	1	1	F7
04	0	0	1	0	0	Shut. State Lgt. Latch	1	1	1	1	1	0	1	1	FB
05	0	0	1	0	1	Unused	1	1	1	1	1	1	1	1	FF
06	0	0	1	1	0	Door Switch Reset Bit	1	1	1	1	1	1	1	0	FE
07	0	0	1	1	1		1	1	1	1	1	1	1	1	FF
08	0	1	0	0	0		1	1	1	1	1	1	1	1	FF
09	0	1	0	0	1		1	1	1	1	1	1	1	1	FF
0A	0	1	0	1	0		1	1	1	1	1	1	1	1	FF
0B	0	1	0	1	1		1	1	1	1	1	1	1	1	FF
0C	0	1	1	0	0		1	1	1	1	1	1	1	1	FF
0D	0	1	1	0	1		1	1	1	1	1	1	1	1	FF
0E	0	1	1	1	0		1	1	1	1	1	1	1	1	FF
0F	0	1	1	1	1		1	1	1	1	1	1	1	1	FF
10	1	0	0	0	0		1	1	1	1	1	1	1	1	FF
11	1	0	0	0	1		1	1	1	1	1	1	1	1	FF
12	1	0	0	1	0		1	1	1	1	1	1	1	1	FF
13	1	0	0	1	1		1	1	1	1	1	1	1	1	FF
14	1	0	1	0	0		1	1	1	1	1	1	1	1	FF
15	1	0	1	0	1		1	1	1	1	1	1	1	1	FF
16	1	0	1	1	0		1	1	1	1	1	1	1	1	FF
17	1	0	1	1	1		1	1	1	1	1	1	1	1	FF
18	1	1	0	0	0	Interrupt Clr. Slot 0	1	1	1	1	1	1	0	1	FD
19	1	1	0	0	1	Interrupt Clr. Slot 1	1	1	1	1	1	1	0	1	FD
1A	1	1	0	1	0	Interrupt Clr. Slot 2	1	1	1	1	1	1	0	1	FD
1B	1	1	0	1	1	Interrupt Clr. Slot 3	1	1	1	1	1	1	0	1	FD
1C	1	1	1	0	0	Interrupt Clr. Slot 4	1	1	1	1	1	1	0	1	FD
1D	1	1	1	0	1	Interrupt Clr. Slot 5	1	1	1	1	1	1	0	1	FD
1E	1	1	1	1	0	Interrupt Clr. Slot 6	1	1	1	1	1	1	0	1	FD
1F	1	1	1	1	1	Interrupt Clr. Slot 7	1	1	1	1	1	1	0	1	FD

Laser Shutter Controller
Address Decoder Prom A

Taking the signals in alphabetic order, their function can easily be seen. The Interlock Latch Control signal (A) is an active low signal that is used to latch the 8-bit shutter state into an output latch/driver. The data are actually latched synchronously by the E clock signal after the correct address for this latch has been decoded (i.e. confirmed) by the PROM and the

74HCT679. The logic equation for this signal shows that it is a write operation with latching occuring on the falling edge of the E clock.

The Shutter Latch Control signal (B) and the Shutter State Output Lights Latch Control signal (D) are similarly generated. When the correct address for these latch/drivers are detected, the 8-bit data is written in synchronization with the E clock. The first of these signals controls the on/off bits that ultimately open and close shutters and the second controls LEDs that indicate to the user whether shutters are open or closed.

The last control signal is the Shutter State Buffer Read Enable signal (C). This signal differs slightly from the other three because it is a read operation and not a write. This signal, like the others, is active low and is controlled by the E clock. This signal, however, is activated during a microprocessor read instead of a write.

The function of this signal is to allow a read operation to occur from an 8-bit buffer that continuously monitors the actual state of the laser safety shutters. Through the use of external circuitry (such as photodetectors) logic levels are generated and applied to the inputs of the buffer. During an emergency shutter closure, the microprocessor reads this buffer to determine if the shutters actually closed and then takes appropriate action.

2.2.1.3 SLOT CARD DECODING

The slot card address decoding is performed similar to the decoding scheme employed for the I/O ports. A 74S288 PROM is configured as one-fourth of a 5-line-to-32-line decoder/demultiplexer and its 8 data lines are used to enable 1 of 8 slot cards (see figure 5). This PROM is in parallel with the I/O port PROM and acts as the next highest 8 lines of the 32-line decoder.

Unlike the I/O ports, the slot card data are buffered from the microprocessor bus. To accommodate this, the decoding scheme for the slot cards must include control signals to effect data transfers between the slot cards and the microprocessor. The first of these signals is the Slot

Card Tristate Enable signal. This signal is produced by performing a logical NAND on the select signals from the PROM and then NANDing this result with the appropriate control signals from the microprocessor. The actual logic function is given in equation 8.

$$\text{Slot Card Tristate Enable} = \overline{(\text{E Clock} \cdot R/\overline{W}) \cdot F}$$
$$\text{Where } F = \overline{S_0 \cdot S_1 \cdot S_2 \cdot S_3 \cdot S_4 \cdot S_5 \cdot S_6 \cdot S_7} \qquad (8)$$

This signal is active low. To make this signal active, both the E clock and the read/write signal from the microprocessor must be logic high. This ensures synchronized access on a read from the CPU. In addition, one of the select lines from the PROM must be low (i.e., a slot card is being addressed). If both of these conditions are met, the Slot Card Tirstate Enable signal will be active. This will allow the buffers that separate the slot card data bus from the microprocessor bus to be enabled.

Although not shown in figure 5, the Slot Card Interrupt Bus is actually pulled high through a series of 1 KΩ resistors. This is done to ensure good logic level high signals to the slot cards when in the inactive state.

A second control signal used for slot card control is the Clear Slot Card Interrupt signal. This signal is used to reset the slot cards after an interrupt is serviced. This active low signal is derived from the microprocessor's control signals and one of the data lines from the I/O port decoding PROM. The data line from this PROM (specifically, data line D2 from PROM A) is one that is unused in the decoding scheme for the I/O ports and it is active low each time a clear signal is to be sent to a slot card. This signal is generated when one of the eight addresses for clearing the slot cards is active ($0098 - $009F) and when the E clock synchronizes during a write cycle to one of these locations. The logic function for this signal is given in equation 9 and the schematic is figure 6.

$$\text{Clear Slot Card Interrupt} = \text{PROM A(D2)} + \overline{E \cdot R/\overline{W}} \qquad (9)$$

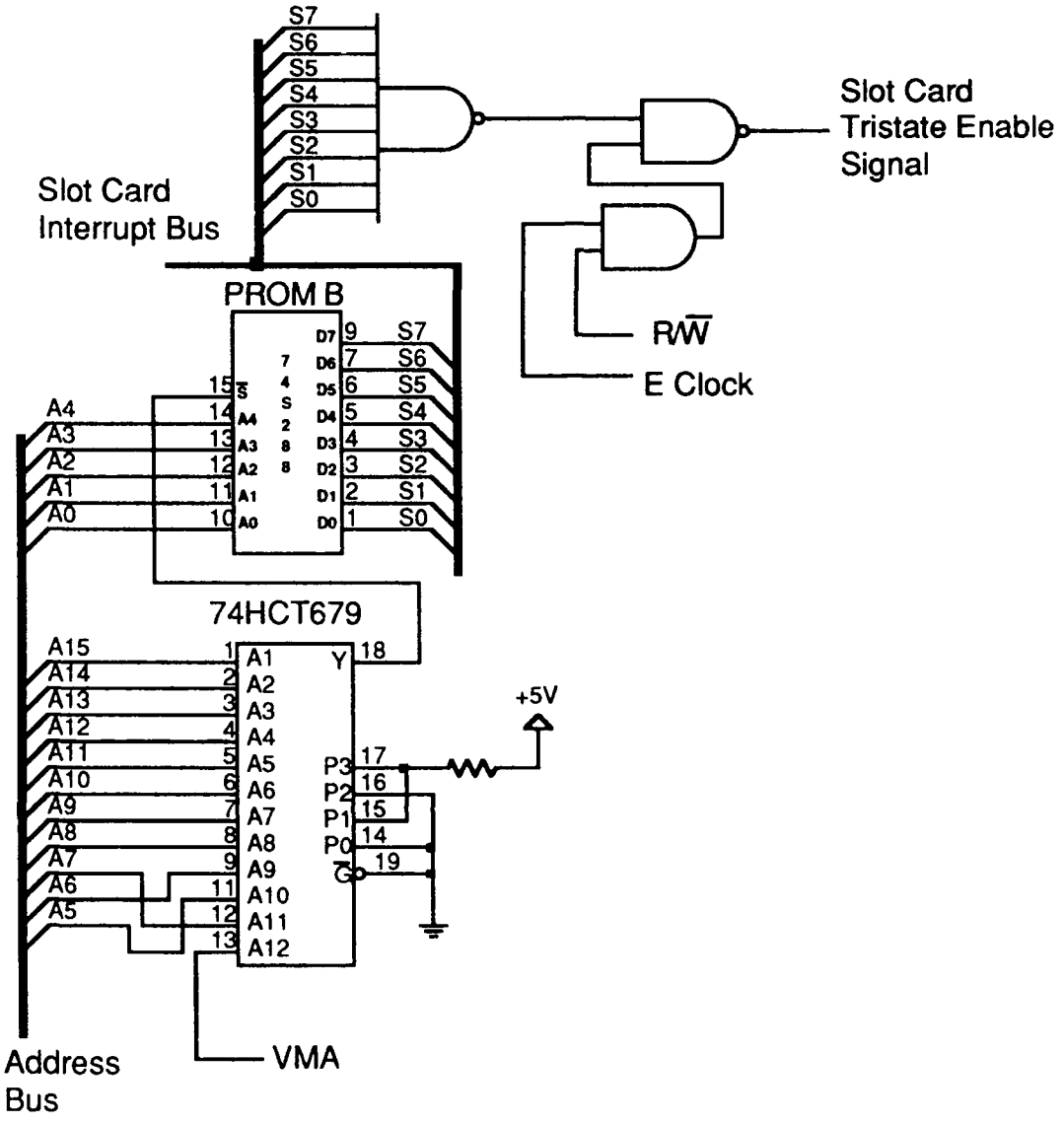


FIGURE 5 - Slot Card Decoding

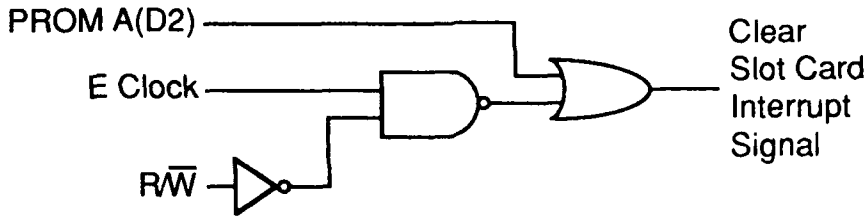


FIGURE 6 - Slot Card Interrupt Clear Circuit

The PROMs used in the decoding scheme for both the I/O ports and the slot cards are not exclusively independent. Since they are both strictly in parallel, they both become active for the same range of addresses. However, the bit patterns in these PROMs are arranged so that only one device is active on the bus at any given time. The analogy to a 5-line-to-32-line decoder/demultiplexer is not strictly correct because clear signals sent to the slot cards will cause two data lines (one from each PROM) to become active at the same time. In all other respects, however, the two PROMs do function collectively as one-half of a 5/32 decoder.

2.2.1.4 OTHER CONTROL SIGNALS

There are two other signals generated by address decoding methods within the laser shutter controller. One of theses signals is used to reset the NMI input circuitry and the other is used to control data switching between the slot cards and the microprocessor. Each of these signals will be discussed when the circuitry for the NMI Reset and the slot card buffer bus is discussed.

2.2.2 THE MICROPROCESSOR DATA BUS

The microprocessor data bus is an 8-bit parallel bus that connects to the I/O ports, the system software EPROM and the buffer circuit to the slot cards. All information passed to and

from the various elements of the laser shutter controller travels over this bus. As with other Motorola 6800-based microprocessors, the data transfer on the the data bus is synchronized with the E clock signal. The cycle time for data bus transfers is one period of the E clock. The information on the data bus becomes available during a read or write operation during the logic high portion of the E clock. Latching of the data on the bus occurs on the falling edge of the E clock.

When interfacing to the slot card buffers or the I/O ports, the data bus functions bidirectionally. Operation instructions can be received from the slot cards over the data bus as can laser shutter status information from one of the I/O ports. Write operations from the microprocessor over the data bus include opening and closing shutters, reseting slot cards and changing the state of the laser shutter status indicator lights.

In addition to serving as a pathway for data to and from the slot card buffers and I/O ports, the data bus also serves to transport the system software instructions to the MC6802. All instructions fetched and executed by the microprocessor are delivered over the data bus. As opposed to the I/O ports, data bus operations between the microprocessor and the system EPROM are strictly read operations.

2.2.3 THE SLOT CARD BUFFER BUS

The slot card buffer bus (circuitry shown in figure 7) is a secondary data bus used mainly for data transfers between the microprocessor data bus and the slot cards. This bus is isolated from the microprocessor data bus by tri-state data selectors. This bus is connected to half of the data lines of the data selectors and they are connected to the microprocessor data bus when the select line is in the proper logic state. The other half of the data lines to the data selectors are either tied to logic zero or are connected to two status signals that are read by the MC6802. One Status signal is the Interrupt Verify Signal from the slot cards and the other is a signal indicating the status of the doors in the lab.

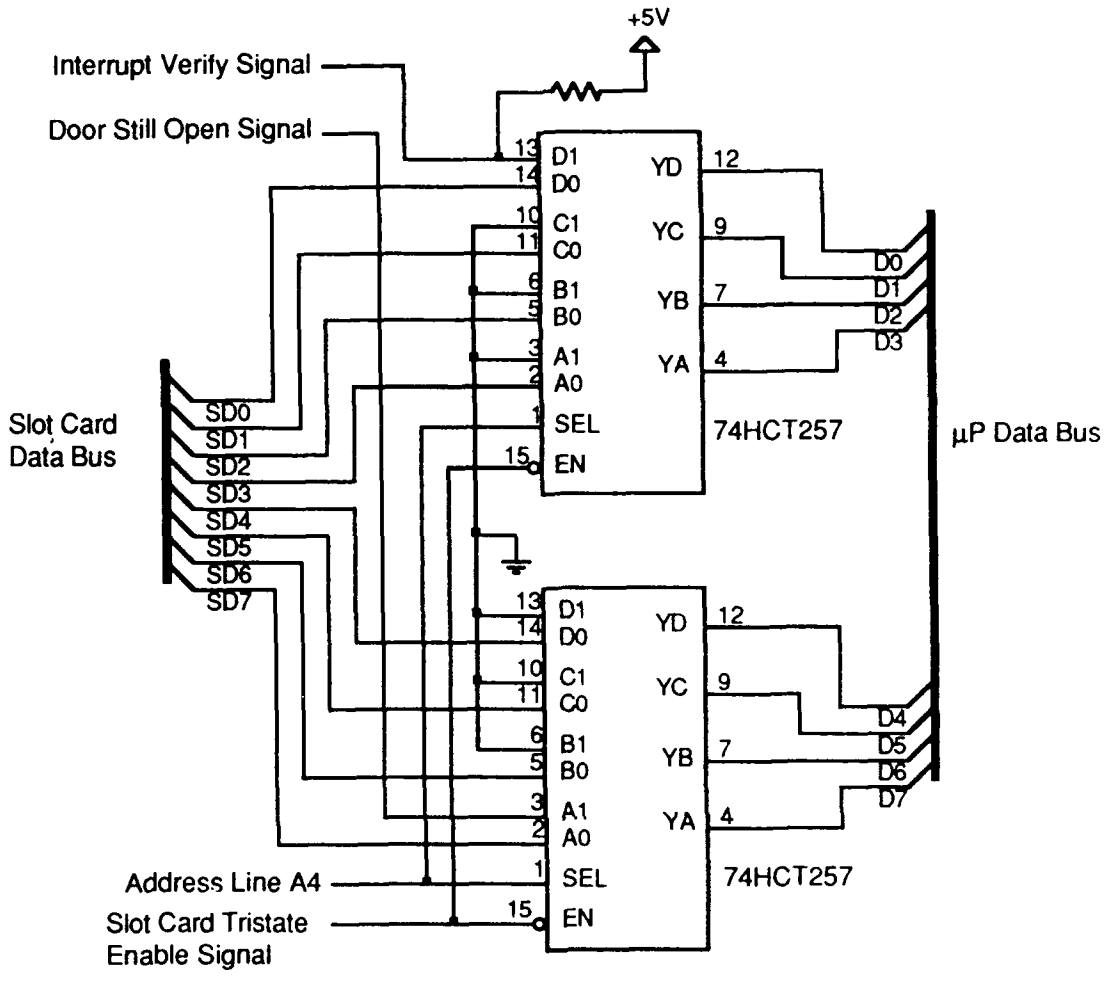


FIGURE 7 - Slot Card Bus Buffers

Specifically, the slot card bus buffers are comprised of two 74HCT257 Quad 2-Line to 1-Line Data Selectors/Multiplexers. These multiplexers route data or slot card status information (and door status information) to the microprocessor data bus during an interrupt service. The 74HCT257 has separate control lines for both output enable and data selection. The microprocessor controls both of these lines during and interrupt service to a slot card. The select line is connected directly to address line A4 and the logic level of this line determines whether slot card data or status information will be routed to the microprocessor data bus. When A4 is high, the

MC6802 is accessing either status information from the slot cards or the status of the laboratory doors. When A4 is logic low, the microprocessor is reading command data from the slot cards.

TABLE 3 - Slot Card Bus Buffer Data

A4	D0	D1	D2	D3	D4	D5	D6	D7
0				*Slot Card Data Bus*				
1	A	0	0	0	0	0	0	B

A = Interrupt Verify Signal
B = Door Still Open Signal

It should be noted that the decoding for this select line (i.e., A4 only) does not provide for mutually exclusive accessing of the slot cards. There are many valid addresses that can cause selection between slot card data and status information. This, however, is unimportant since this information can only appear on the microprocessor data but when the output enable lines of the multiplexers are active. This signal, called the Slot Card Tristate Enable Signal is decoded mutually exclusively to the slot cards and can only be activated by very specific addresses.

It is important to note that the door status signal can be read while reading any of the slot card status signals. This poses no conflict since the slot card status and the door status are on different data lines of the bus. The microprocessor simply masks out the bits that are of no interest at the time and tests only that bit that is important.

2.3 THE NONMASKABLE INTERRUPT CIRCUIT

The nonmaskable interrupt circuit is at the heart of the safety features of the shutter controller. This circuit, though simple in design, provides signals to the rest of the system that are vital for all safety aspects of the shutter controller. This circuit serves two critical functions. First, it unconditionally interrupts the system when a breach of the laboratory is detected. Second, It continoulsy monitors the entrances to the lab area in order to prevent the system from allowing shutters to open when the lab area is not secure.

A schematic of the circuit is shown in figure 8. The circuit has three inputs and two outputs. The first output is the nonmaskable interrupt signal to the microprocessor. When this signal is at logic low, the MC6802 is forced into a priority service routine. This routine closes all laser shutters, tests to ensure that all of the shutters did indeed close and then monitors the entrances to the lab to prevent any shutters from opening until the area is once again secure.

The second output from the circuit is the door status signal. This signal, called the Door Still Open signal, is used by the microprocessor to determine if the lab entrances are still open. A logic low on this signal indicates that lab entrances are still unsecure and the microprocessor allows no further action to be taken until all entrances are secure.

Of the three inputs, the most important is the door switch input. This input is connected to a series of magnetic reed switches that are located at the entrances of the lab. When the entrances are secure, the reed switches are closed and a logic low is on this input. An open lab entrance causes this signal to go high, and the nonmaskable interrupt circuit causes the microprocessor to take action.

The other two inputs to this circuit are reset inputs and they are used to place the nonmaskable interrupt circuit in an initial state. These two inputs are wired-OR to the same location in the circuit using diodes. The common connection to the diodes is tied logic high through a pullup resistor so that either of the two inputs can cause resetting of the circuit.

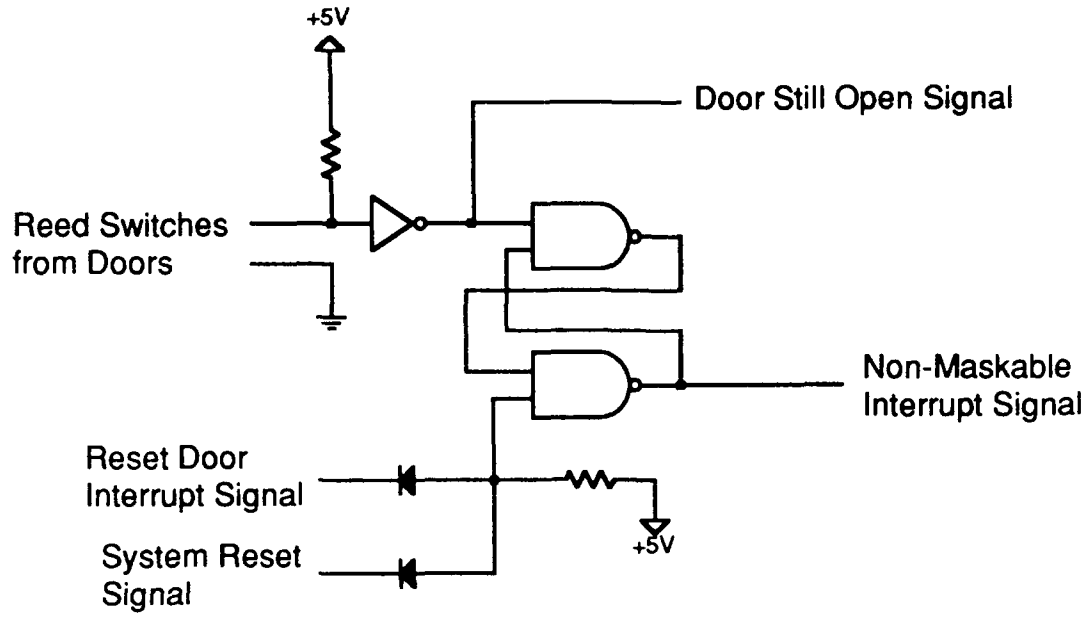


FIGURE 8 - NonMaskable Interrupt Circuit

The first of these two inputs is the system reset input. This input ensures that the circuit is not inadvertently interrupting the MC6802 upon reset. When the system is first turned on, or during a manual reset, this signal goes low causing the nonmaskable interrupt signal to be a logic high. This ensures that there are no unwanted interrupts upon reset. The second input is a reset signal that the microprocessor sends after it has determined that the lab area is once again secure after a breach.

2.4 THE SYSTEM RESET CIRCUIT

The system reset circuit is shown in figure 9. This circuit is responsible for bringing the laser shutter controller into an initialized operating state. This occurs automatically during power-up of the system or it can be initiated manually by the operator when required. Reset is accomplished by holding the reset pin of the MC6802 (pin 40) at a logic level low for a required time duration. During power-up conditions, this duration is not less than 100 milliseconds. If

during normal operation a manual reset is required, the reset pin must be held low at least three CPU clock cycles. Using a 3.58-MHz crystal (divided by 4 internal to the MC6802) the clock cycle is 1.12 µS. The reset pulse duration during a manual reset must therefore be at least 3.36 µS long.

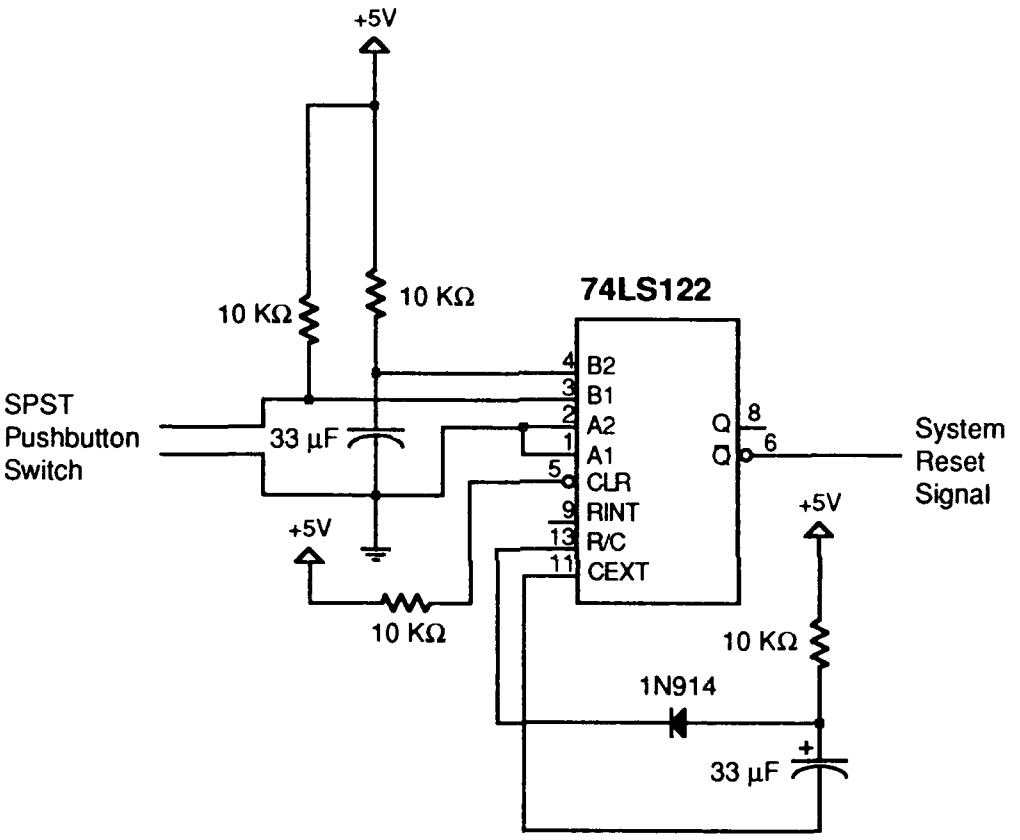


FIGURE 9 - System Reset Circuit

The circuit is designed around a 74LS122 retriggerable monostable multivibrator. The 74LS122 has 4 triggerable inputs (A1, A2, B1, B2) with two of the inputs (B1, B2) having Schmitt trigger hysteresis. As can be seen in figure 9, the 74LS122 is configured to trigger both from power-up and from a manual push button switch. Upon power-up the 74LS122 is allowed to become stable before a reset is triggered. This is accomplished by driving one of the B inputs (B2) with a series RC network. Although the hysteresis threshold voltage is not stated in the data

information for the 74LS122, a reasonable value for the threshold can be assumed to be the minimum input high voltage level given for the device (i.e., 2 volts). Discounting the minimal loading effects on the RC network by the B input, the wait period for stablizing the 74LS122 is given by equation 10.

$$t = -(RC)\ln(\frac{3}{5}) \text{ Seconds} \qquad (10)$$

Taking the values of R and C from figure 9 (10KΩ and 33 μF) the wait time before sending a reset pulse to the system is about 169 mS.

Once this wait period has expired the 74LS122 generates a pulse at its outputs with a duration governed by equation 11.

$$t = 0.33RC \text{ Seconds} \qquad (11)$$

Using the values for R and C connected between pins 11 and 13 of the 74LS122 yields a pulse duration of about 109 mS. This time plus the wait time given in equation 10 is more than adequate to cause a valid reset of the MC6802 during a power-up sequence.

A manual reset is initiated by causing a logic low to appear on pin 3 (B1) of the 74LS122 during normal operation. When activated, this will cause the 74LS122 to generate a pulse whose duration is given in equation 11. This will immediately cause the microprocessor to halt operation and self-initialize.

As indicated previously, for this reset, the MC6802 requires a low reset pulse with a duration that is at least three clock cycles long. With a 3.58-MHz crystal, the cycle time is about 1.12 μS so that a reset pulse longer than 3.36 μS will cause a valid reset. The time given in equation 11 far exceeds this requirement.

In addition to initializing the microprocessor, the reset from the 74LS122 also initializes and temporarily inhibits the nonmaskable interrupts from the lab entrance switches. This

is done to prevet contention between NMI and reset during the initialization. This also ensures that the NMI circuit is in a known state so that no valid laboratory breaches will be missed.

2.5 THE INPUT/OUTPUT PORTS

The Input/Output (I/O) ports are a set of 8-bit latches, drivers and buffers that serve to transfer information between the laser shutter controller and the external world. The I/O ports serve to drive both the actual shutters and interlocks as well as the indicator lights that reflect the shutters' status. In addition, the I/O ports provide the means to obtain feedback from the shutters to indicate if closure occurred at the proper time.

The actual configuration of the I/O ports is shown in figure 10. The ports consist of three DP8311 Octal Latch/Drivers and a 74HCT541 Tri-state Octal Buffer. The latches provide for control of the interlocks, laser shutters and status lights while the octal buffer is the input port for determining the actual state of the shutters. The DP8311 latch is 8-bits wide and has NPN transistor open collector outputs. These latches are capable of driving loads such as small lights or LEDs as well as mini-relays. As used in the shutter controller, the DP8311 latches drive both LEDs and relays.

The 74HCT541 is a TTL-LS compatible CMOS buffer. This buffer is 8-bits wide and has tri-state output enable control. This buffer gives the microprocessor access to external circuitry that indicates the actual state of the safety shutters. Under normal conditions, a shutter that is physically open will cause a logic low to appear on one of the input lines to the buffer. If a shutter is closed, a logic high will appear. During an emergency close operation, (i.e., a door to the lab has been opened) the microprocessor closes all of the shutters and then reads this port to determine the actual status of the shutters. If a logic low is detected anywhere on this port, the system assumes a fault occurred and all lasers are turned off by opening the interlocks.

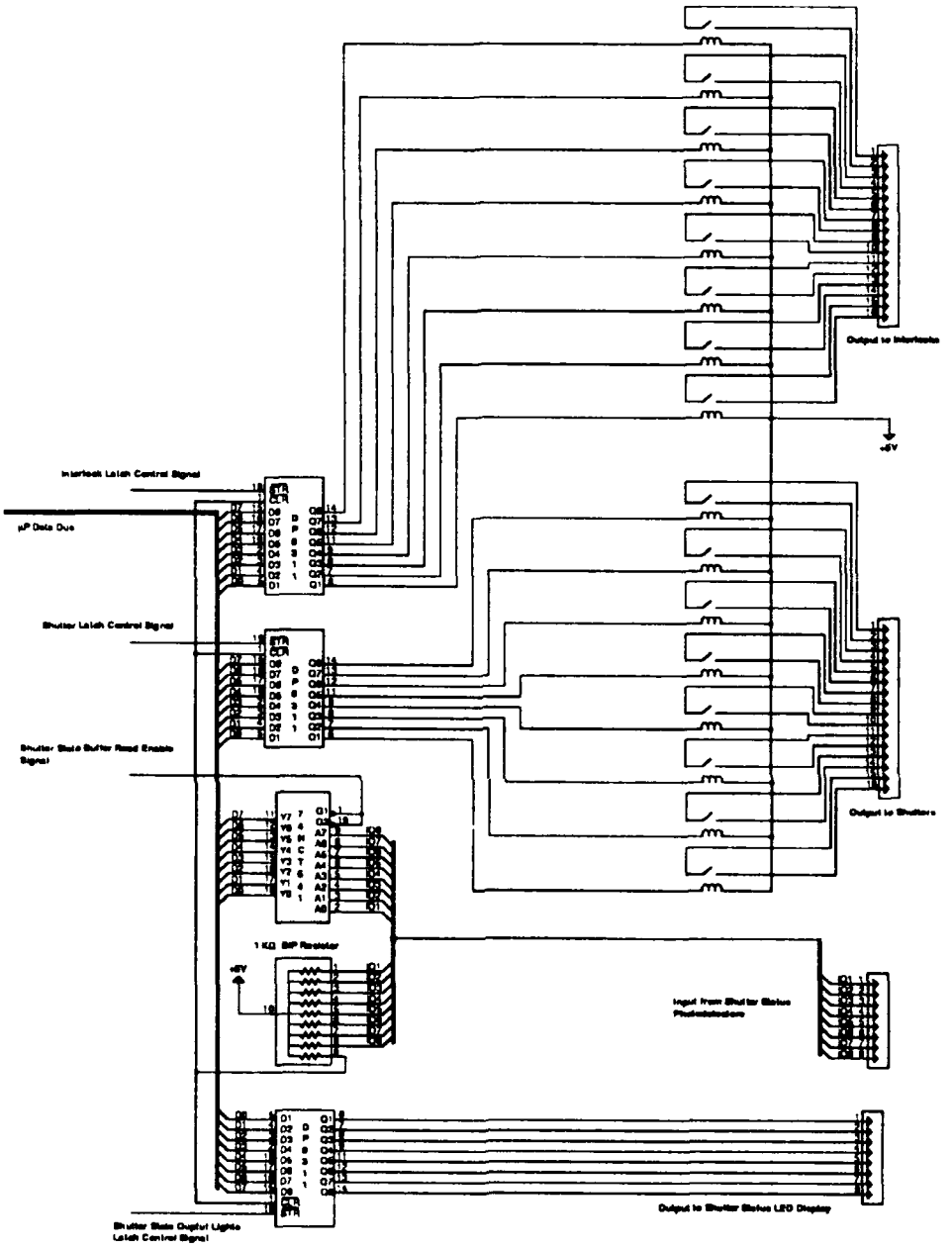


FIGURE 10 - The Input/Output Ports

As output ports, the DP8311 latches are not capable of handling heavy loads. While they are ideal for LED and small light control, they are not meant to drive larger loads such as those associated with shutter systems. In addition, they don't offer a great deal of flexibility to future interfaces (i.e., something other than shutters). To increase flexibility and loading capability, the DP8311 latches driving the shutters and interlocks are interfaced to small SPST relays. These relays in-turn can be used to control programmable power supplies for driving shutters and can be used directly to control the interlocks. In addition, the use of these relays provides a control mechanism that is both isolated and polarity independent.

3.0 THE SLOT CARDS

To provide a versatile interface between the external lab environment and the laser shutter controller, a set of plug-in slot cards has been developed. These cards plug into a backplane and interface with the controller to allow the user to conveniently control the shutters and interlocks. These cards enable the user to open and close the shutters and interlocks through the use of push button switches, infrared remote controls and through computer interfaces.

Within the system, each slot card is an independent device. With limited exceptions, each card can be programmed to control any shutter or interlock attached to the laser shutter controller. In fact, more that one card can be legitimately configured to control the same shutter or interlock. In addition, the cards are interchangeable. Any card can be placed in any slot allowing the user to mix and match card types easily. This type of open-ended versatility provides the user with maximum flexibility to allow tailoring of the shutter controller system to a specific lab environment.

3.1 SLOT CARD COMMON FEATURES

All slot cards plugged into the system are in parallel. However, due to the tristate buffering scheme employed, only one card at a time is actively interfaced with the system. The parallelism of the slot cards allows all of the interrupt lines from all cards to be tied to the same interrupt line of the system. Each slot card has a common collector interrupt driver and they are all connected to the MC6802's IRQ input. At this input the lines are pulled to a logic high state by a 10 KΩ resistor. Any card (and potentially more than one card at a time) can cause this line to go low requesting service from the processor. During an interrupt service, the microprocessor polls each slot card, in turn, to determine which card is requesting service.

All slot cards have an interrupt verify signal and an interrupt clear signal that are connected to the microprocessor data bus through tristate buffers. The interrupt verify signal is read by the system sequentially from lowest slot to highest slot to determine which card is interrupting the system. This signal becomes active on the microprocessor data bus when the specific address for a particular card is addressed by the MC6802. The interrupt clear signal is generated by the system to clear a slot card after an interrupt has been serviced. While this signal appears in parallel to all of the slot cards, only the slot card whose specific address is being accessed sees the signal. This allows more than one card to send valid interrupts at the same time.

Additionally within the system, all slot cards have a data bus that is common but separated by tristate buffers. All commands sent by the slot cards to the system pass from this bus to the microprocessor data bus when a specific address is activated. As is the case with other signals, this facilitates multiple and simultaneous interrupts to occur.

The hardware configuration present on all slot cards that allows each to be in parallel yet separate is the slot card interrupt priority level DIP switch. This switch consists of eight separate single-pole-single-throw (SPST) inputs all tied together on one side. The microprocessor places a successive logic low on these SPST switches in order to activate the buffers isolating the two data buses. The key to isolation is to ensure that each of the slot cards has all but one unique SPST switch open. In effect, this allows the microprocessor to poll each successive slot, activating only one card at a time to service any interrupts.

For all eight potential slot cards, there are a total of 24 addresses that can access the cards. There are eight each for data access, interrupt verification and interrupt clearing (3 for each slot). These can be found in the memory map of figure 2.

The slot cards request a specific action from the controller by providing an 8-bit command code during an interrupt request. These codes, shown in table 4, cause the controller to open or close individual shutters or interlocks or collectively open or close all shutters or interlocks. In addition, one code is provided to allow reset of the entire system from a slot card.

TABLE 4 - Interrupt Request Action Table

	Interrupt Card Data	HEX	Shutter Cont. Action to Take	Data Out from Cont.	HEX
0	0000 0000	00	Branch to Reset	N/A	N/A
1	0000 0001	01	Unused	N/A	N/A
2	0000 0010	02	Unused	N/A	N/A
3	0000 0011	03	Unused	N/A	N/A
4	0000 0100	04	Close Shutter #1	1111 1110	FE
5	0000 0101	05	Open Shutter #1	0000 0001	01
6	0000 0110	06	Close Shutter #2	1111 1101	FD
7	0000 0111	07	Open Shutter #2	0000 0010	02
8	0000 1000	08	Close Shutter #3	1111 1011	FB
9	0000 1001	09	Open Shutter #3	0000 0100	04
10	0000 1010	0A	CloseShutter #4	1111 0111	F7
11	0000 1011	0B	Open Shutter #4	0000 1000	08
12	0000 1100	0C	Close Shutter #5	1110 1111	EF
13	0000 1101	0D	Open Shutter #5	0001 0000	10
14	0000 1110	0E	Close Shutter #6	1101 1111	DF
15	0000 1111	0F	Open Shutter #6	0010 0000	20
16	0001 0000	10	Close Shutter #7	1011 1111	BF
17	0001 0001	11	Open Shutter #7	0100 0000	40
18	0001 0010	12	Close Shutter #8	0111 1111	7F
19	0001 0011	13	Open Shutter #8	1000 0000	80
20	0001 0100	14	Close Interlock #1	0000 0001	01
21	0001 0101	15	Open Interlock #1	1111 1110	FE
22	0001 0110	16	Close Interlock #2	0000 0010	02
23	0001 0111	17	Open Interlock #2	1111 1101	FD
24	0001 1000	18	Close Interlock #3	0000 0100	04
25	0001 1001	19	Open Interlock #3	1111 1011	FB
26	0001 1010	1A	Close Interlock #4	0000 1000	08
27	0001 1011	1B	Open Interlock #4	1111 0111	F7
28	0001 1100	1C	Close Interlock #5	0001 0000	10
29	0001 1101	1D	Open Interlock #5	1110 1111	EF
30	0001 1110	1E	Close Interlock #6	0010 0000	20
31	0001 1111	1F	Open Interlock #6	1101 1111	DF
32	0010 0000	20	Close Interlock #7	0100 0000	40
33	0010 0001	21	Open Interlock #7	1011 1111	BF
34	0010 0010	22	Close Interlock #8	1000 0000	80
35	0010 0011	23	Open Interlock #8	0111 1111	7F
36	0010 0100	24	Close All Shutters	N/A	N/A
37	0010 0101	25	Open All Shutters	N/A	N/A
38	0010 0110	26	Close All Interlocks	N/A	N/A
39	0010 0111	27	Open All Interlocks	N/A	N/A

Table 4, shows 37 individual code commands that are available for use. There are 32 separate "local" commands for opening or closing individual shutters or interlocks, 4 "global"

commands for opening or closing all shutters or interlocks and one command for resetting the system.

When a valid command is sent to the controller, a specific action is taken. In the case of a "local" command, the controller will perform a logical AND or OR of the current state of the shutters or interlocks with the proper bit pattern to effect the desired change. With "global" commands, the controller will simply write a bit pattern to the shutters or interlocks to open or close them all. In the case of the reset command, the system performs a branch to the beginning of the system monitor software.

There are currently two types of cards that can be used with the laser shutter controller. The first is a manual switch card that allows the user to open and close shutters (or interlocks) by means of push button switches placed in close proximity to the laser system. The second card is an infrared remote control card that allows the user to open and close shutters via a hand held transmitter. Each will be discussed in detail.

3.2 THE MANUAL SWITCH CARD

The schematic for the Manual Switch card is shown in figure 11. This card provides the capability of manual activation of shutters or interlocks. The card has two inputs for SPST switches that allow the user to send one of two code commands to the controller. In the most common configuration, pressing one switch will send the command to open a shutter and pressing the other switch will send the command to close a shutter.

On the card, two sets of DIP switches allow the user to program which commands will be sent to the controller. While normally the two distinct commands to open and close a particular

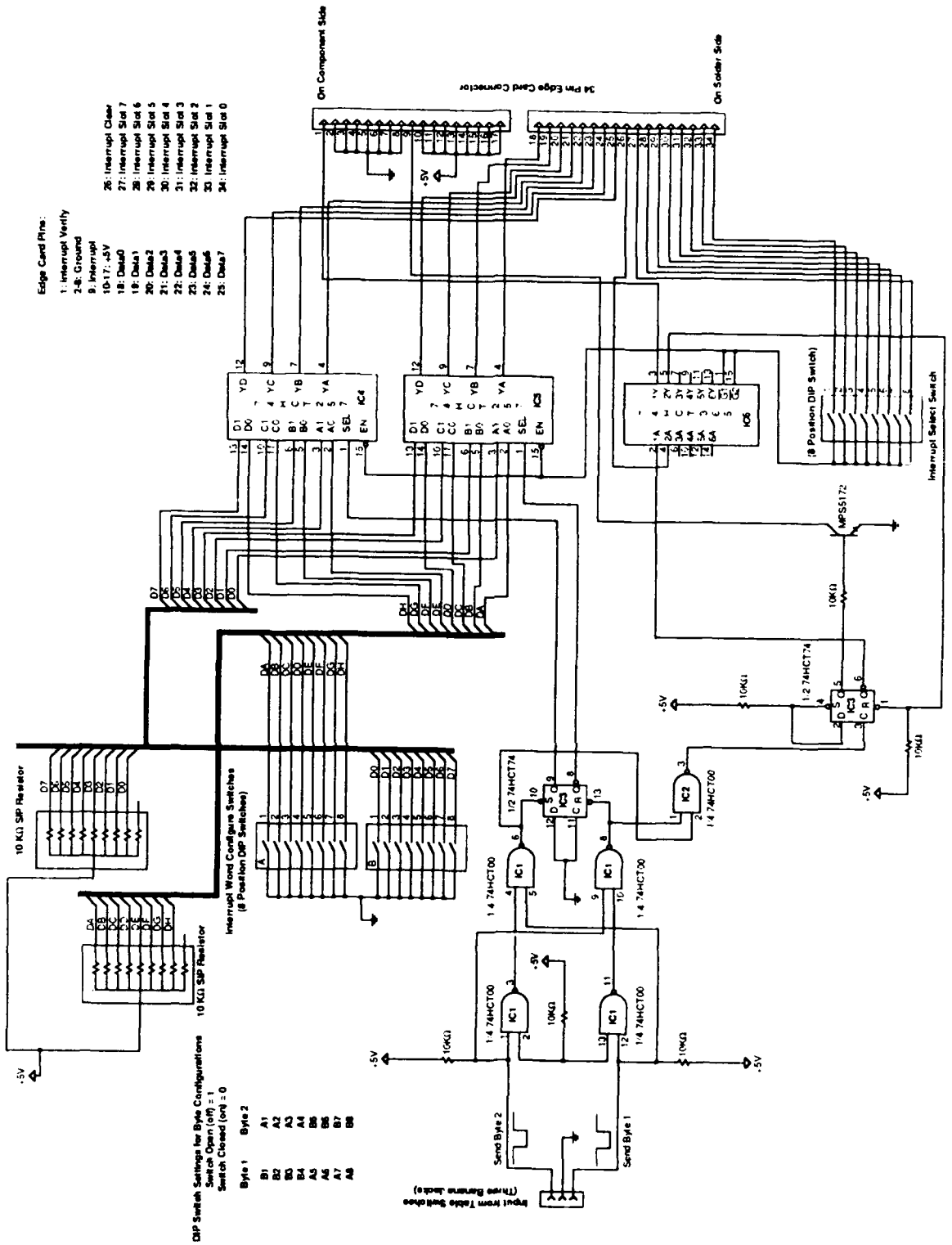


FIGURE 11 - Manual Switch Card

shutter are programmed using these switches, the user can choose any two commands (or for that fact any one command) that is listed in table 4.

When used to control a shutter, the interface usually consists of a series of SPST switches placed around an optical table near the laser system. Half of these switches are in parallel and are connected to one of the inputs of the card. The other half are also in parallel and are connected to the other input of the card. Pressing one switch opens a shutter, pressing the other closes a shutter. This provides the laser user with a convenient way to control the laser light when setting up or performing an experiment.

The input section of the manual switch card is shown in figure 12, and its operation is relatively straightforward. With low logic level signals being provided by SPST switches connected to In1 and In2, the circuit provides a smooth transition between the selection of two command words. When the switches pull either In1 or In2 low, the set or reset lines of D flip-flop FF1 with go low respectively. This causes the Q and Q prime outputs of this flip-flop to toggle between logic states to select either one or the other command byte programmed into the manual switch card. Regardless of which command word is selected, making either In1 or In2 low will cause the output of NAND3 to go logic high. This causes FF2 to clock through the logic high at its D input to the Q output. This turns on the NPN transistor causing the interrupt line to the microprocessor to become active. In other words, each time either switch is pressed the circuit will select the proper command word for output and notify the system that a service is requested.

The remaining circuitry for the manual switch card consists of the tri-state buffers and multiplexers that transfer the command data and other signals between the card and the rest of the system. These tri-state devices are controlled by signals generated by the system in response to an interrupt generated by the manual switch card.

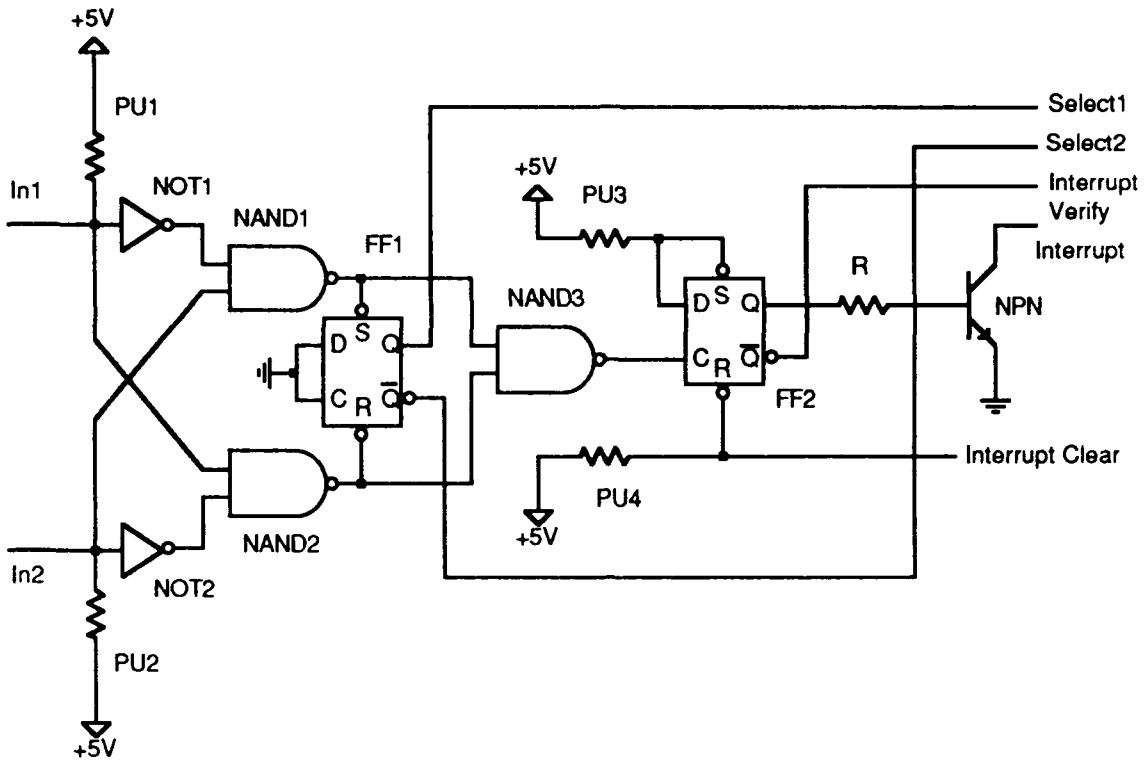


FIGURE 12 - Manual Switch Card Input Section

3.3 THE INFRARED REMOTE CONTROL INTERFACE

The infrared (IR) remote control interface consists of two parts. The first part is a hand held unit that allows the user to open and close certain shutters from a remote location. The second part is the slot card receiver that interprets the commands sent by the remote unit and directs the shutter controller to take action. Each of these will be discussed separately.

In the present configuration, only two shutters can be controlled by IR remote. These are shutters one and two whose on and off codes (given in table 4) are binary 4,5,6 or 7. Future modifications to the shutter controller system will provide the capability to remotely send any of the 37 commands given in table 4 by IR remote.

3.3.1 THE INFRARED REMOTE TRANSMITTER UNIT

The infrared transmitter is designed around the National Semiconductor LM1871 RC Encoder/Transmitter integrated circuit. The LM1871 is intended for use in radio frequency remote control of toys such as hobby aircraft but is easily adaptable to an IR transmission scheme. The device employs a type of pulse width encoding to relay information. Pulses of varying widths are sent in a train to the receiving device where the duration of the pulses are used to control some action. Usually the pulses are integrated to provide a voltage which is used to drive a servo motor (as is the case with hobby-type toys). As employed in this IR transmitter, the width of each pulse is of little importance. Instead, the information to be sent is encoded in the number of transmitted pulses.

The LM1871 allows three to six independent commands (channels) to be sent per transmission. The number of channels transmitted is determine by a two-bit binary word with the number of channels sent being 3, 4, 5 or 6. This type of information encoding may loosely be called pulse number encoding, and this scheme is perfect for control of two independent shutters (on_1, off_1, on_2, off_2).

While the LM1871 is designed to be a complete encoder/transmitter, only the encoding function is used in the IR transmitter (see figure 13). A typical encoded ouput from the LM1871 is shown in figure 14. One complete transmission is accomplished in the time period T_f called the frame time. The actual information (when pulse width encoding) is relayed in the time period T_{ch} with the time between channels being denoted by T_m. T_m and T_f are fixed using resistor/capacitor combinations with the durations given by the following equations.

$$T_m = 0.69R_mC_t \tag{12}$$

$$T_f = 1.1R_fC_f + T_m \tag{13}$$

The pulse duration for the channel time T_{ch} is governed by an equation like that for the modulation time T_m.

$$T_{ch} = 0.69R_{ch}C_t \tag{14}$$

Since there are six channels, there are usually six independent values for R_{ch}. In hobby toys, this is usually accomplished by a six-potentiometer joystick. The IR transmitter does not use the pulse widths to encode the information but rather the pulse number. Tf, Tm and Tch are all fixed. It should be noted the T_{ch} and T_m are both governed by the same timing capacitor C_t.

In order to help ensure error-free transmission, the pulse number encoded information is interrupted-carrier modulated (ICM) onto a 40-KHz carrier. This amounts to turning the 40 KHz carrier on and off depending on the logic level of the modulating signal. This eliminates false triggering at the receiving device due to changes in the ambient room light. The carrier frequency of 40 KHz was chosen as a matter of convenience to allow the use of a commercially available IR receiver/demodulator. Most IR transmitters (such as those used with home entertainment equipment) ICM modulate at the commercial AM intermediate frequency (IF) of 455 KHz. Using carriers in this frequency range usually requires the transmitter and receiver to be tuned circuits thus increasing their complexity. The justification for using carriers with frequencies this high involves the number of commands to be sent. Home entertainment systems usually require a relatively large number of commands to control all of the user functions. In order to keep the transmission time small (~mS) the carrier frequency must be made large. This problem is not encountered with this laser shutter remote control since only four commands exist.

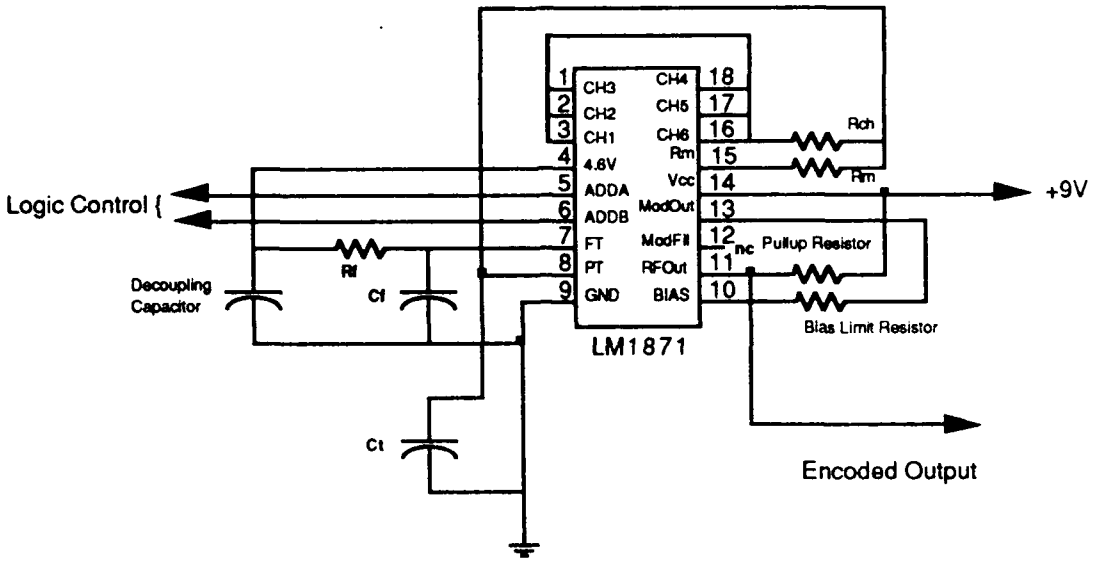


FIGURE 13 - The Command Encoder

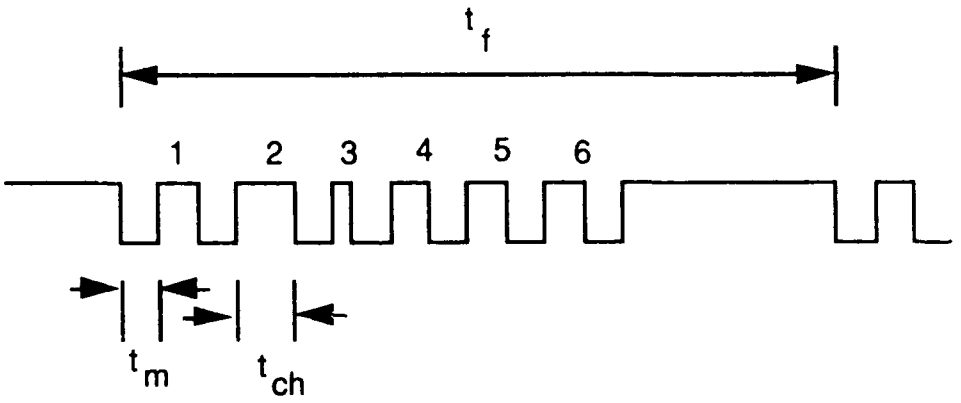


FIGURE 14 - Typical Command Signal

For this IR transmitter, ICM modulation is accomplished by gating an oscillator on and off (see figure 15). This produces a 40-KHz pulse train enveloped by the command pulses generated from the LM1871. This signal is then used to drive an infrared emitting diode. The oscillator is an astable logic oscillator that employs a resistor/capacitor network to control the oscillation frequency. The frequency of oscillation is roughly governed by the following equation.

$$F_{osc} = \frac{1}{2R_1C\left(\frac{0.405R_2}{R_1+R_2} + 0.693\right)} \qquad (15)$$

The internal capacitances of the NAND gates affects the frequency of oscillation somewhat and some tuning is required.

As can be seen in figure 15, the encoded command from the LM1871 is used to gate the oscillator on and off to produce an enveloped 40-KHz squarewave. This signal is applied to the base of an NPN transistor which in turn drives the IR light emitting diode (IR LED). The current through the IR LED is limited to about 100 mA peak, and this provides sufficient power to transmit about 15 feet.

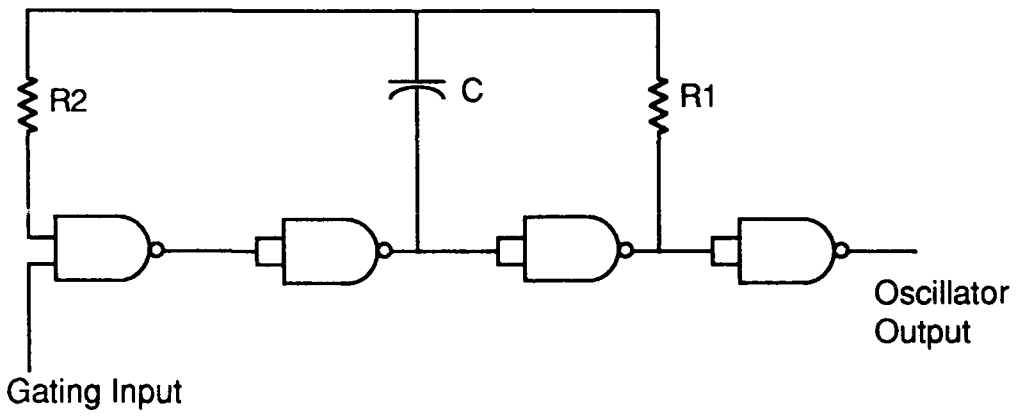


FIGURE 15 - The Carrier Oscillator

Since the remote control must be a mobile unit, it is battery operated. To conserve power and substantially lengthen battery life, the remote only draws power when a command is sent. This is achieved by gating the current from the battery through a PNP transistor. The transistor is turned on (i.e., power applied) only when one of the command switches is closed (see figure 16). At the same time that the power is applied, the logic levels that determine the number of channels to be transmitted is set. The number of channels to transmit and the application of

power is controlled by the array of diodes connected to the command switches. The diodes act as an isolating logic

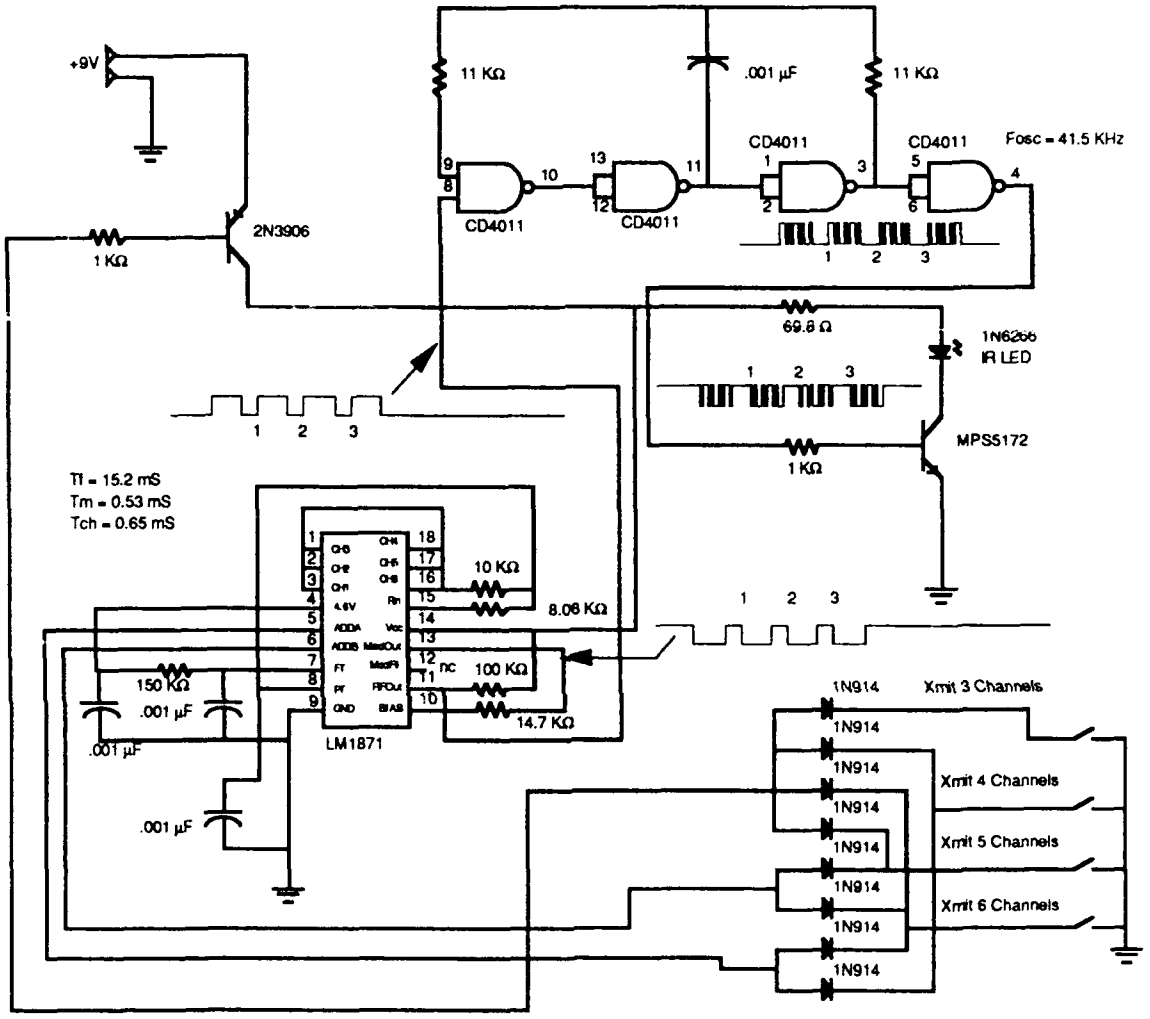


FIGURE 16 - The IR Transmitter Circuit

interpreter for the switches performing the dual functions of encoding the command logic while isolating each switch from the others.

3.3.2 THE REMOTE DECODER SLOT CARD

The remote decoder slot card serves as a receiver and interpreter for the commands sent by the IR remote transmitter unit. This card performs two specific functions each time a command is detected from the transmitter. First, since the pulses coming from the transmitter are asynchronous, the receiver must first determine the beginning of a frame for a command. After the correct frame of reference is determined, the card must then ensure that the command being sent is of a valid nature. To meet these requirements, the remote decoder follows an alogrithm.

Since the incoming information is contained in the number of the incoming pulses the alogrithm neccessarily includes a counting function. To ensure that the pulse train being counted is valid, two consecutive pulse trains must be received that have the same number of pulses. In addition, only a particular range of pulse counts is valid (namely 4,5,6 or 7) so any values above these numbers are ignored. In addition, valid incoming pulse trains are very regular in spacing and duration, so the remote decoder also uses this property to exclude spurious noise and ensure a valid signal.

To perform the required tasks for detection and decoding, the remote decoder card, shown in figure 17, employs a series of digital timing and counting functions. At the heart of the decoder is a dual set of counters comprised of 74HCT193 synchronous binary counters and a 74123 dual retriggerable one shot. The incoming signal is first detected and demodulated by a commercial IR detector module (Sharp GP1U52X) to produce a series of TTL level pulses that can be counted. Upon receiving the first pulse of the train, the remote decoder starts a timer (i.e., one-half of the 74123) that allows the pulse train to be routed to a 74HCT193 binary counter. This timer is configured to produce a gating pulse at its Q output (pin 13) whose duration is about 3 ms. This

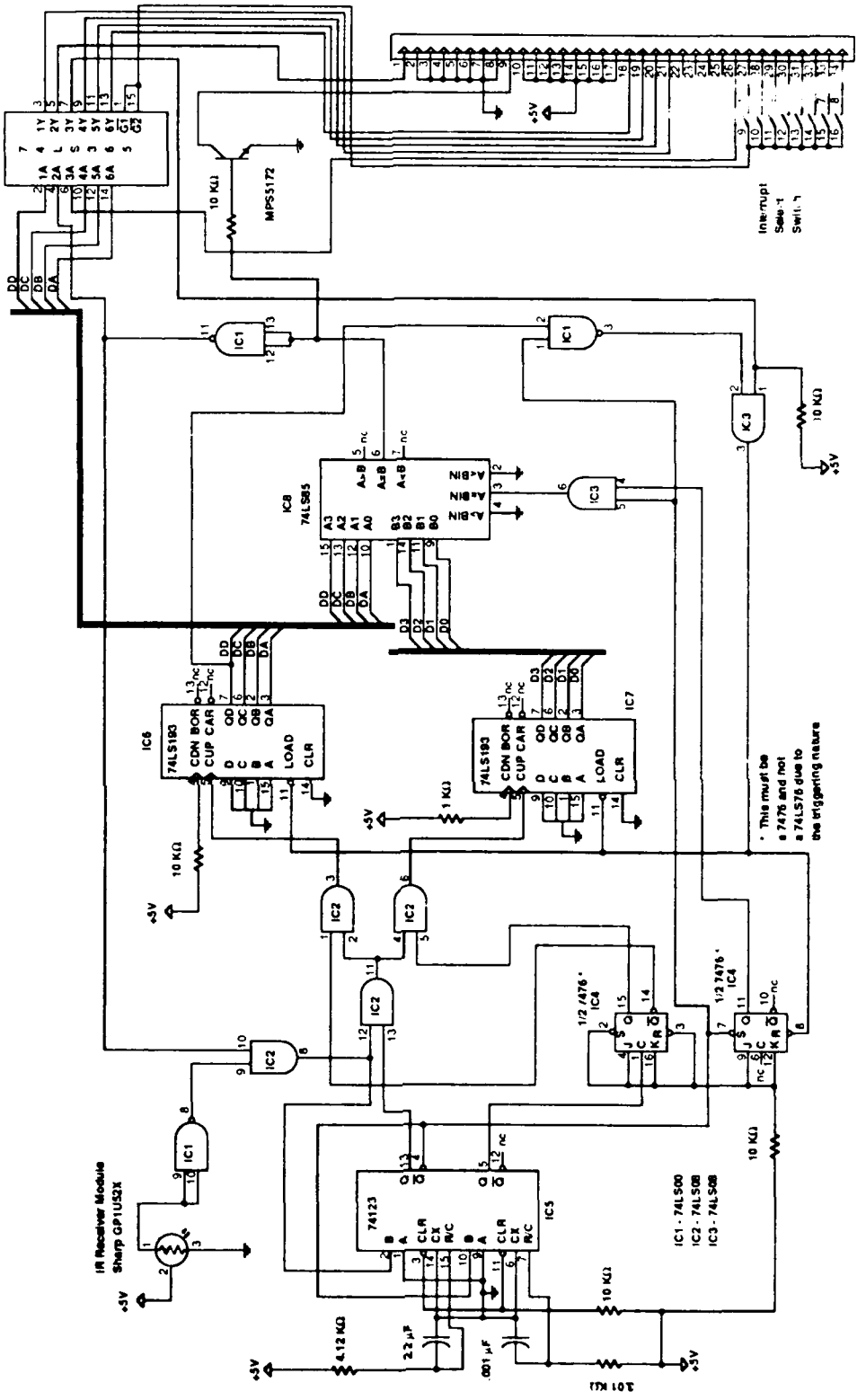


FIGURE 17 - The IR Remote Decoder

duration is slightly longer than the duration of a valid pulse coming from the IR transmitter. As long as pulses coming into the remote decode are at intervals shorter that the duration of this timer, they will be routed to the counter. If this doesn't occur, the 74123 will time out. This causes a 7476 flip-flop to toggle states which in-turn causes any subsequent pulses to be routed to the second counter. This allows two consecutive commands to be received by the remote decoder, each being counted by a different counter. This toggling action goes back and forth first activating one counter and then the other for each train of pulses received. This interaction between the pulses the timer and the counters ensures that erratic or spurious signals will not be viewed as legitimate commands.

Assuming that a valid pulse train is being received by the remote decoder, the circuit will operate in this fashion. As the pulse train comes in, the 74123 timer will gate the pulses through to the first 74193 counter where the total number will be accumulated. At the end of this valid train of pulses, the timer will time-out triggering the second one-shot on the 74123 (output at pin 5). This causes the 7476 flip-flop to toggle states at pins 14 and 15. This will cause any subsequent train of pulses to be routed to the second 74193 counter. If the next pulse train coming in is valid and if it is identical to the preceeding pulse train, the total number of counts accumulated by the second counter will equal the total accumulated by the first counter. This condition indicates that a valid signal has been received by the remote decoder.

To determine when two consecutive pulse trains are equal, the remote decoder employs a 4-bit magnitude comparator (74HCT85). After each complete pulse train is received, the contents of both counters are compared. If they are equal, the remote decoder card sends an interrupt request to the shutter controller. At the same time, the gate input that allows the incoming pulse train to reach the counters is disabled. This prevents any further commands from the IR transmitter from reaching the decoder card until the current interrupt is completed.

In order to prevent spurious interrupts from occurring due to possible counting glitches, the comparator is only activated at the completion of each successive pulse train. This is

accomplished by gating the timing pulse from the one shot through a NAND gate to the A=B control input of the 74HCT85 comparator.

In order to synchronize the frame reference, one of the counters' most significant bit is used to reset both counters to a known state when the count value exceeds the maximum valid value (i.e., seven). Since the initial state of the counters cannot be guaranteed, it is conceivable that no two consecutive commands would ever cause the counters to be equal. However, the feedback from the counter ensures that the counters will start from an initialized state.

The rest of the circuitry on the remote decoder card is essentially the same as for other slot cards. A tristate buffer system interfaces to the shutter controller with an open collector interrupt driver. As with the other slot cards, the tristate bus is controlled by signals from the shutter controller.

4.0 FUTURE ENHANCEMENTS

The laser shutter controller system functions very well in its present form; however, there are a series of changes and modifications that will be made to future implementations of the system. First, a possible redesign to the microprocessor system may be made. The MC6802 and some of the associated decoding and I/O ports may be replaced with the single-chip microcomputer of the MC68701. This microcomputer chip contains the MC6800 microprocessor with 2K of EPROM and 128 bytes of internal RAM for stack operations all on a single integrated circuit. In addition, the MC68701 can be configured to have I/O ports on board thus eliminating the need for external I/O port circuitry. Making this change to the system will greatly reduce the chip count of the processor section of the controller making it more compact.

A second change to the system will be a redesign of the infrared remote transmitter and receiver section. The changes here will involve the use of a different transmission and reception scheme to allow IR control of all possible system commands. While the present configuration is perfectly adequate (i.e., control of two shutters), increased capabilities will allow for greater expansion and flexibility for future use.

Additional changes to the system may include minor reworking of the manual slot card to allow easier command word selection but this is not critical. A more important future development will be the addition of a digital interface card to allow shutter system control from personal computers. A straightforward 8-bit interface to PCs will allow shutter system control to be added to other program control such as those used for experimentation.

5.0 SYSTEM SCHEMATICS

(Figures 18 through 22)

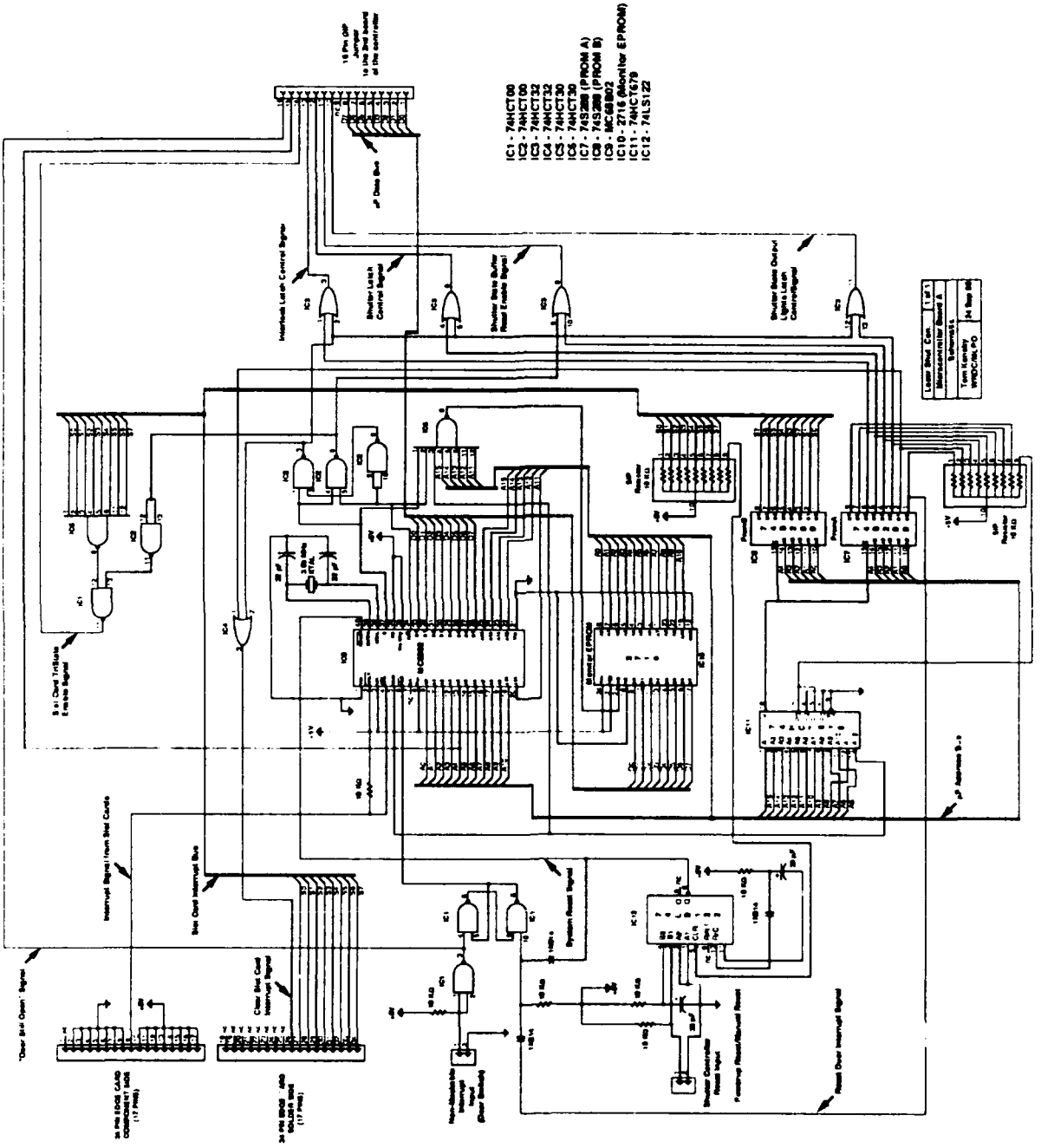


FIGURE 18 - Microcontroller A Schematic

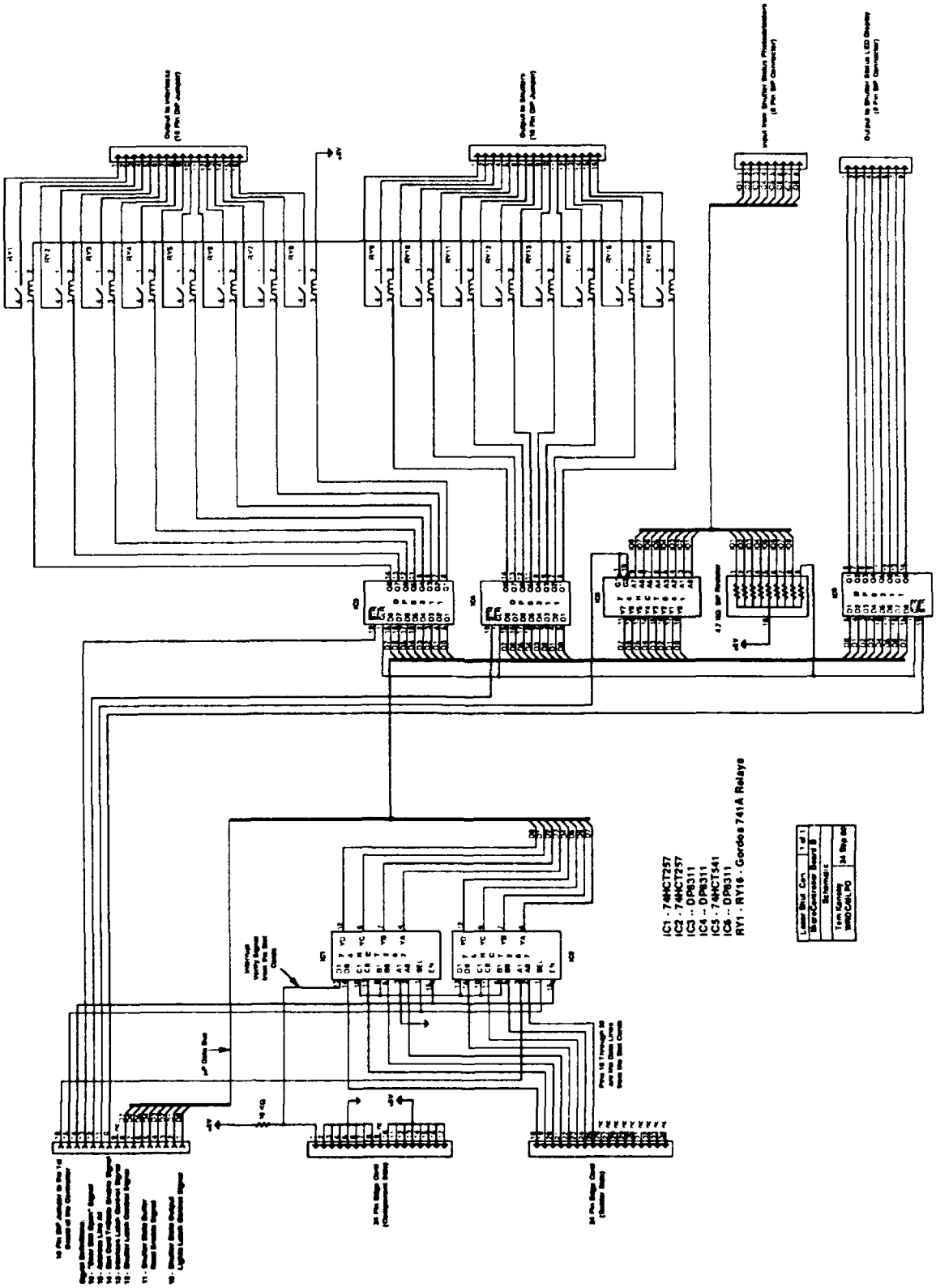


FIGURE 19 - Microcontroller B Schematic

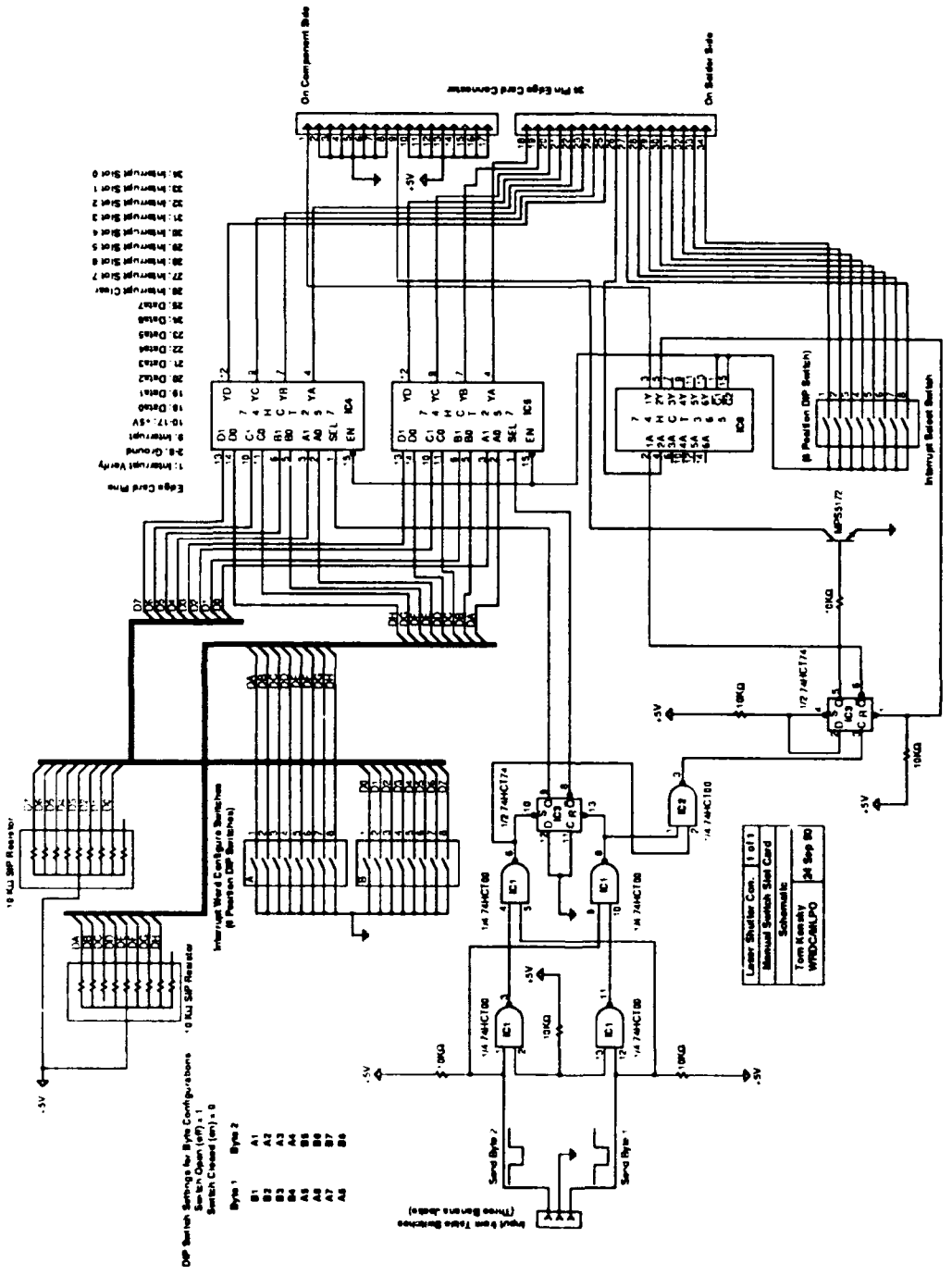


FIGURE 20 - Manual Switch Card Schematic

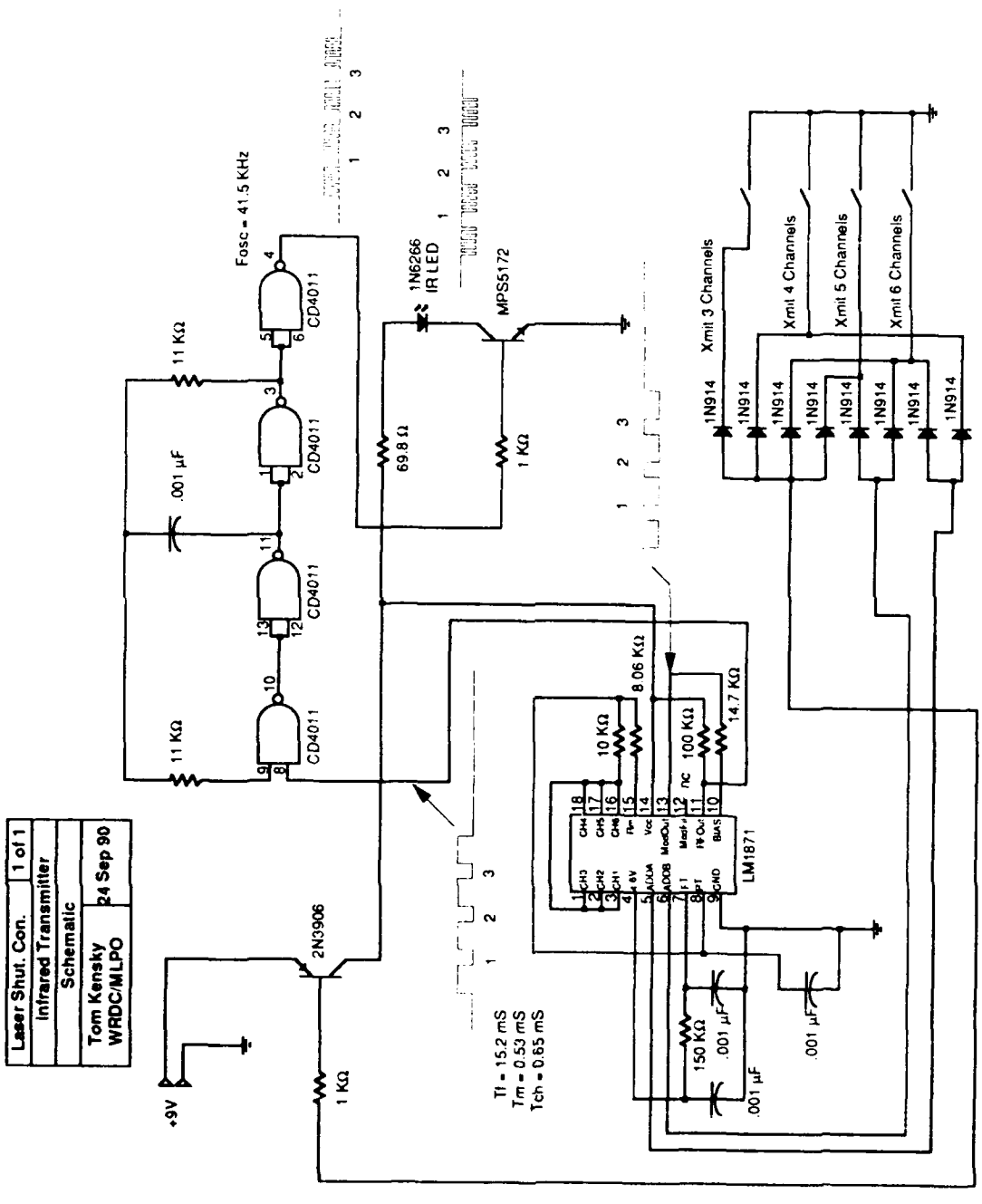


FIGURE 21 - IR Remote Transmitter Schematic

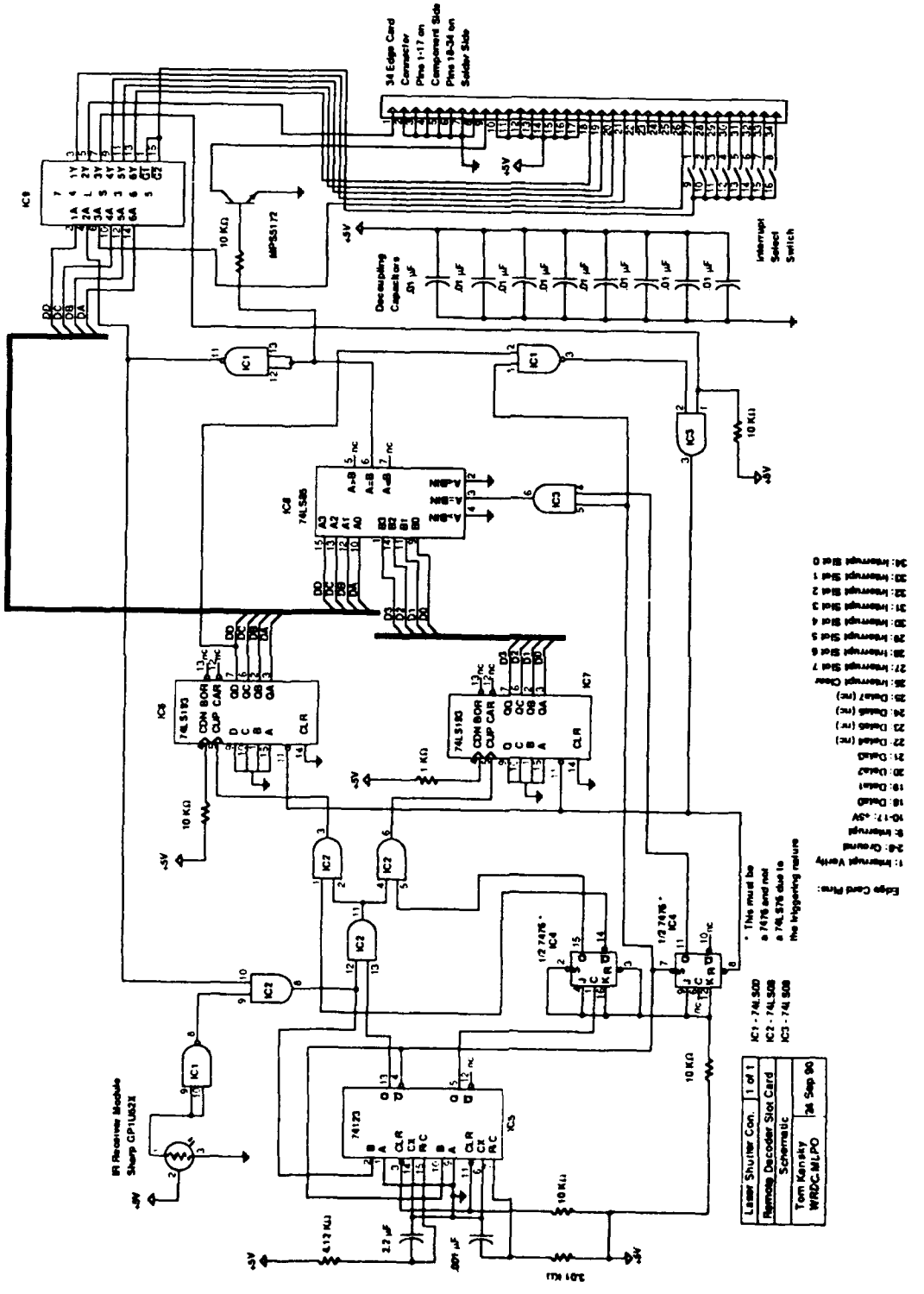


FIGURE 22 - IR Remote Receiver Card Schematic

6.0 SYSTEM SOFTWARE

RESET ROUTINE

MEM. MAP ADDR.	EPROM ADDR.	HEX CODE	LABEL	OPERATION	OPERAND	COMMENTS
F800	0000	0F	INITIALIZE:	SEI		Disable IRQ and SWI interrupts
F801	0001	8E 00 7F		LDS	#$7F	Set stack at top of internal RAM (007F)
F804	0004	4F		CLRA		Load Acc. A with 0's
F805	0005	97 82		STAA	$82	Close all shutters
F807	0007	97 84		STAA	$84	Turn off Shutter State LED's (all shutters closed)
F809	0009	97 0B		STAA	$0B	Store current shutter status in location $000B
F80B	000B	86 FF		LDAA	#$FF	Load Acc. A with 1's
F80D	000D	97 81		STAA	$81	Close all interlocks (enable all lasers)
F80F	000F	97 0A		STAA	$0A	Store current interlock status in location $000A
F811	0011	97 98		STAA	$98	Reset Interrupt Card in slot 0
F813	0013	97 99		STAA	$99	Reset Interrupt Card in slot 1
F815	0015	97 9A		STAA	$9A	Reset Interrupt Card in slot 2
F817	0017	97 9B		STAA	$9B	Reset Interrupt Card in slot 3
F819	0019	97 9C		STAA	$9C	Reset Interrupt Card in slot 4
F81B	001B	97 9D		STAA	$9D	Reset Interrupt Card in slot 5
F81D	001D	97 9E		STAA	$9E	Reset Interrupt Card in slot 6
F81F	001F	97 9F		STAA	$9F	Reset Interrupt Card in slot 7
F821	0021	0E	BEGIN:	CLI		Enable maskable interrupts
F822	0022	3E		WAI		Wait for occurence of interrupt
F823	0023	20 FC		BRA	BEGIN	All interrupts return to this line

NON-MASKABLE INTERRUPT ROUTINE

MEM. MAP ADDR.	EPROM ADDR.	HEX CODE	LABEL	OPERATION	OPERAND	COMMENTS
F825	0025	0F	NMI:	SEI		Disable all maskable interrupts
F826	0026	4F		CLRA		Load Acc. A with 0's
F827	0027	97 82		STAA	$82	Close all shutters
F829	0029	97 84		STAA	$84	Turn off Shutter State LED's (all shutters closed)
F82B	002B	97 0B		STAA	$0B	Update current shutter status
F82D	002D	8D 41		BSR	DELAY	Branch to the Time Delay Subroutine
F82F	002F	96 83		LDAA	$83	Read Shutter Status port
F831	0031	81 FF		CMPA	#$FF	See if all shutiers are closed
F833	0033	27 05		BEQ	CHKDOOR	If all shutters are closed see if door is still open
F835	0035	4F		CLRA		Load Acc. A with 0's
F836	0036	97 81		STAA	$81	All shutters didn't close; turn off all lasers
F838	0038	97 0A		STAA	$0A	Update current interlock status
F83A	003A	96 90	CHKDOOR:	LDAA	$90	Read door status
F83C	003C	85 80		BITA	#$80	Bit test MSB of Acc. A for a logic 0
F83E	003E	27 FA		BEQ	CHKDOOR	Door is still open; keep testing until closed
F840	0040	97 86		STAA	$86	Reset the door switch input
F842	0042	0E		CLI		Enable all interrupts
F843	0043	3B		RTI		Return from the NMI interrupt

INTERRUPT REQUEST ROUTINE

MEM. MAP ADDR.	EPROM ADDR.	HEX CODE	LABEL	OPERATION	OPERAND	COMMENTS
F844	0044	0F	IRQ LOOP:	SEI		Disable further IRQ interrupts
F845	0045	CE 00 90		LDX	#$0090	Load index register with lowest slot card address
F848	0048	A6 00	SLOTTEST:	LDAA	(00),X	Read Interrupt Verify Bit
F84A	004A	85 01		BITA	#$01	Check LSB for a logic 0
F84C	004C	27 08		BEQ	CONTINUE	Branch if a valid interrupt was detected
F84E	004E	08		INX		If not then increment index register
F84F	004F	8C 00 98		CPX	#$0098	Check to see if all slots have been read
F852	0052	26 F4		BNE	SLOTTEST	If not go back and read next slot
F854	0054	20 18		BRA	OUT	If last slot was read then get out of IRQ
F856	0056	DF 00	CONTINUE:	STX	$00	**********
F858	0058	96 01		LDAA	$01	** These lines subtract 8 from the **
F85A	005A	80 08		SUBA	#$08	** Index Register in order to allow *
F85C	005C	97 01		STAA	$01	** the data from the interrupting **
F85E	005E	DE 00		LDX	$00	** card to be read **
F860	0060	A6 00		LDAA	(00),X	**********
F862	0062	8D 1A		BSR	IRQACT	Goto IRQ Action Subroutine
F864	0064	96 01		LDAA	$01	**********
F866	0066	8B 10		ADDA	#$10	** These lines add 16 to the Index **
F868	0068	97 01		STAA	$01	** Register in order to allow **
F86A	006A	DE 00		LDX	$00	** theslot crad to be reset **
F86C	006C	A7 00		STAA	(00),X	**********
F86E	006E	0E	OUT:	CLI		Enable all interrupts
F86F	006F	3B		RTI		Go Back and wait for another interrupt

TIME DELAY SUBROUTINE

MEM. MAP ADDR.	EPROM ADDR.	HEX CODE	LABEL	OPERATION	OPERAND	COMMENTS
F870	0070	4F	DELAY:	CLRA		Clear Acc. A
F871	0071	5F		CLRB		Clear Acc. B
F872	0072	4C	MINORLOOP:	INCA		Increment Acc. A by 1
F873	0073	81 FF		CMPA	#$FF	Compare Acc. A to $FF (255)
F875	0075	26 FB		BNE	MINORLOOP	Go back if the count hasn't reached 255
F877	0077	4F		CLRA		Clear Acc. A
F878	0078	5C	MAJORLOOP:	INCB		Increment Acc. B by 1
F879	0079	C1 0A		CMPB	#$0A	Compare Acc. B to $0A (10)
F87B	007B	26 F5		BNE	MINORLOOP	Go back if count hasn't reached 10
F87D	007D	39		RTS		Return from subroutine

IRQ ACTION SUBROUTINE

MEM. MAP ADDR.	EPROM ADDR.	HEX CODE	LABEL	OPERATION	OPERAND	COMMENTS
F87E	007E	CE FD 00	IRQACT:	LDX	#$FD00	Load Index Reg. with start Addr. of Action Table
F881	0081	DF 10		STX	$10	Store Addr. in locations $10 and $11
F883	0083	97 11		STAA	$11	Make effective address $FDXX
F885	0085	DE 10		LDX	$10	Load Index Register with Addr. of Action Table
F887	0087	81 24		CMPA	#$24	Is it a CLOSE ALL SHUTTERS command?
F889	0089	27 4A		BEQ	CLSALLSHUT	Go to CLOSE ALL SHUTTERS routine
F88B	008B	81 25		CMPA	#$25	Is it an OPEN ALL SHUTTERS command?
F88D	008D	27 4F		BEQ	OPALLSHUT	Go to OPEN ALL SHUTTERS routine
F88F	008F	81 26		CMPA	#$26	Is it a CLOSE ALL INTERLOCKS command?
F891	0091	27 55		BEQ	CLSALLINT	Go to CLOSE ALL INTERLOCKS routine
F893	0093	81 27		CMPA	#$27	Is it an OPEN ALL INTERLOCKS command?
F895	0095	27 59		BEQ	OPALLINT	Go to OPEN ALL INTERLOCKS routine
F897	0097	81 00		CMPA	#$00	Is it a RESET command?
F899	0099	27 5C		BEQ	GOBACK	If so then go back and reset
F89B	009B	81 04		CMPA	#$04	**********
F89D	009D	25 5B		BCS	FINISH	These 4 lines make sure that the int. card data
F89F	009F	81 23		CMPA	#$23	is valid (between $04 and $23)
F8A1	00A1	22 57		BHI	FINISH	**********
F8A3	00A3	81 14		CMPA	#$14	Interrupt data was valid and if it is less than $14
F8A5	00A5	25 16		BCS	SHUTSERV	it is a SHUTTER SERVICE command
F8A7	00A7	85 01	INTSERV:	BITA	#$01	Z will be set if LSB of Interrupt Data is a 0
F8A9	00A9	27 08		BEQ	CLOSEINT	If so then it is a CLOSE INTERLOCK command
F8AB	00AB	96 0A	OPENINT:	LDAA	$0A	Get current interlock status
F8AD	00AD	A4 00		ANDA	(00),X	AND with Action Table value to open interlock

MEM. MAP ADDR.	EPROM ADDR.	HEX CODE	LABEL	OPERATION	OPERAND	COMMENTS
F8AF	00AF	97 0A		STAA	$0A	Update current interlock status
F8B1	00B1	20 06		BRA	EXIT1	Go to EXIT1; actual interlocks will be updated
F8B3	00B3	96 0A	CLOSEINT:	LDAA	$0A	Get current interlock status
F8B5	00B5	AA 00		ORAA	(00),X	OR with Action Table value to close interlock
F8B7	00B7	97 0A		STAA	$0A	Update current interlock status
F8B9	00B9	97 81	EXIT1:	STAA	$81	Update actual Interlock Control Latch
F8BB	00BB	20 3D		BRA	FINISH	Prepare to return from interrupt
F8BD	00BD	85 01	SHUTSERV:	BITA	#$01	Z will be set if LSB of Interrupt Data is a 0
F8BF	00BF	27 08		BEQ	CLOSESHUT	If so then it is a CLOSE SHUTTER command
F8C1	00C1	96 0B	OPENSHUT:	LDAA	$0B	Get current shutter status
F8C3	00C3	AA 00		ORAA	(00),X	OR with Action Table value to open shutter
F8C5	00C5	97 0B		STAA	$0B	Update current shutter status
F8C7	00C7	20 06		BRA	EXIT2	Go to EXIT2; actual shutters will be updated
F8C9	00C9	96 0B	CLOSESHUT:	LDAA	$0B	Get current shutter status
F8CB	00CB	A4 00		ANDA	(00),X	AND with Action Table value to close shutter
F8CD	00CD	97 0B		STAA	$0B	Update current shutter status
F8CF	00CF	97 82	EXIT2:	STAA	$82	Update actual Laser Shutter Control Latch
F8D1	00D1	97 84		STAA	$84	Update Shutter Status Light Latch
F8D3	00D3	20 25		BRA	FINISH	Prepare to return from interrupt
F8D5	00D5	4F	CLSALLSHUT:	CLRA		Load Acc. A with 0's
F8D6	00D6	97 82		STAA	$82	Close all shutters
F8D8	00D8	97 84		STAA	$84	Update Shutter Status Light Latch
F8DA	00DA	97 0B		STAA	$0B	Update current shutter status
F8DC	00DC	20 1C		BRA	FINISH	Prepare to return from interrupt
F8DE	00DE	86 FF	OPALLSHUT:	LDAA	#$FF	Load Acc. A with 1's
F8E0	00E0	97 82		STAA	$82	Open all shutters
F8E2	00E2	97 84		STAA	$84	Update Shutter Status Light Latch

MEM. MAP ADDR.	EPROM ADDR.	HEX CODE	LABEL	OPERATION	OPERAND	COMMENTS
F8E4	00E4	97 0B		STAA	$0B	Update current shutter status
F8E6	00E6	20 12		BRA	FINISH	Prepare to return from interrupt
F8E8	00E8	86 FF	CLSALLINT:	LDAA	#$FF	Load Acc. A with 1's
F8EA	00EA	97 81		STAA	$81	Close all interlocks
F8EC	00EC	97 0A		STAA	$0A	Update current interlock status
F8EE	00EE	20 0A		BRA	FINISH	Prepare to return from interrupt
F8F0	00F0	4F	OPALLINT:	CLRA		Load Acc. A with 0's
F8F1	00F1	97 81		STAA	$81	Open all interlocks
F8F3	00F3	97 0A		STAA	$0A	Update current interlock status
F8F5	00F5	20 03		BRA	FINISH	Prepare to return from interrupt
F8F7	00F7	7E F8 00	GOBACK	JMP	INITIALIZE	Return to Reset system
F8FA	00FA	39	FINISH:	RTS		Return from subroutine

ACTION TABLE HEXADECIMAL CODES

MEM. MAP ADDR.	EPROM ADDR.	HEX CODE	COMMENTS
FD04	0504	FE	Close Shutter #1
FD05	0505	01	Open Shutter #1
FD06	0506	FD	Close Shutter #2
FD07	0507	02	Open Shutter #2
FD08	0508	FB	Close Shutter #3
FD09	0509	04	Open Shutter #3
FD0A	050A	F7	CloseShutter #4
FD0B	050B	08	Open Shutter #4
FD0C	050C	EF	Close Shutter #5
FD0D	050D	10	Open Shutter #5
FD0E	050E	DF	Close Shutter #6
FD0F	050F	20	Open Shutter #6
FD10	0510	BF	Close Shutter #7
FD11	0511	40	Open Shutter #7
FD12	0512	7F	Close Shutter #8
FD13	0513	80	Open Shutter #8
FD14	0514	01	Close Interlock #1
FD15	0515	FE	Open Interlock #1
FD16	0516	02	Close Interlock#2
FD17	0517	FD	Open Interlock #2
FD18	0518	04	Close Interlock#3
FD19	0519	FB	Open Interlock #3
FD1A	051A	08	Close Interlock #4
FD1B	051B	F7	Open Interlock #4

MEM. MAP ADDR.	EPROM ADDR.	HEX CODE	COMMENTS
FD1C	051C	10	Close Interlock #5
FD1D	051D	EF	Open Interlock #5
FD1E	051E	20	Close Interlock #6
FD1F	051F	DF	Open Interlock #6
FD20	0520	40	Close Interlock #7
FD21	0521	BF	Open Interlock #7
FD22	0522	80	Close Interlock #8
FD23	0523	7F	Open Interlock #8

6802 INTERRUPT VECTORS

MEM. MAP ADDR.	EPROM ADDR.	HEX CODE	COMMENTS
FFFE:FFFF	07FE:07FF	F8 00	RESET
FFFC:FFFD	07FC:07FD	F8 25	NMI
FFFA:FFFB	07FA:07FB	F8 44	SWI
FFF8:FFF9	07F8:07F9	F8 44	IRQ

6.1 LASER SHUTTER MONITOR SOFTWARE DESCRIPTION

The following description provides details on the operation of the monitor software driving the Laser Shutter Controller.

Reset Routine:

F800 - F823: This section of code performs the initialization required to put the Shutter Controller hardware in a known state. Line F800 disables all maskable interrupts and line F801 sets the top of the microprocessor stack at the highest MC6802 internal RAM location. The stack is used for temporary storage when executing conditional branch instructions during system operation. Lines F805 through F809 ensure that all saftey shutters are closed and that the indicator LED's showing which shutters are open is also properly updated. In addition, a RAM location ($000B) is also updated with the current shutter status (i.e., all closed). This location is used throughout the monitor program for retrieving and updating the state of the shutters. Lines F80B through F80F are used in a similar fashion to initialize and record the state of the laser interlocks. In this case, all interlocks are closed to allow any laser to be turned on. Lines F811 through F81F send interrupt clear commands to all of the plug-in cards to initialize them to a known state. The actual data sent during these commands is irrelevant. Reseting is accomplished through hardware signals and only the address of the write command is important. Lines F321 though F823 finish up the initialization by enabling maskable interrupts (CLI) and waiting or an interrupt. Interrupt services return to line F823 after completion.

Nonmaskable Interrupt (NMI) Routine:

F825 - F843: This routine is invoked whenever the laser work environment is breached (i.e., a door is opened). Line F825 disables all maskable interrupts until completion of this routine. This

does not, however, prevent the occurrence of another NMI. Lines F826 through F82B close all saftey shutters and update the indicator LED's and shutter status memory location. Line F82D then causes a branch to the Time Delay subroutine to allow time for the shutters to all close before testing their actual status. After the delay period is completed, lines F82F through F833 check to see if all of the shutters actually closed. If not, then safety is not ensured and the monitor program turns off all of the lasers by opening their interlocks. This is accomplished in lines F835 through F838. If the test in line F833 determines that all of the shutters actually closed, then normal execution continues at line F83A. From this line through F83E, a bit is tested that indicates if the breached opening is still there (i.e., the door to the lab is still open). The program will not allow any further operation until the breach is secured (i.e., the door is closed). It should be noted that this bit test is performed whether or not the shutters all closed or not. Once the breach is secured, the program enables maskable interrupts and returns for this interrupt routine to line F823.

Interrupt Request (IRQ) Routine:

F844 - F86F: This routine is invoked by the plug-in slot cards. Its function is to affect the shutters and interlocks according to the command byte sent by the plug-in slot cards. This routine provides a convenient way to open and close shutters and interlocks via external commands. These commands are 8-bit words programmed into the plug-in cards and are activated by the user through various means including push button switches, infrared remote control and computer command. Specifically, the IRQ routine takes the command and accesses an action table within the program and performs an operation (e.g., open a particular shutter) according to the code. The IRQ routine begins operation at line F844 by disabling further maskable interrupts. The routine then loads the base address of the plug-in cards ($0090) in the index register and then begins testing each individual card to determine which one sent the interrupt (lines F848 through F854). This is accomplished by bit testing the least significant bit from the plug-in cards (the IRQ verify bit) and then branching when a logic zero is found. If no match is found for any slot, then the

IRQ routine is exited (line F854). If a match is found, execution continues at line F856. This next section (F856 through F860) decrements the index register by eight and reads the actual command being sent by the plug-in card. During this process, the current value of the index register is stored in locations $0000:$0001 for future use. Upon completion of this, the program branches to a subroutine (IRQACT) where the action to the shutters/interlocks is taken (line F862). Upon return the slot card address in locations $0000:$0001 is incremented by 16 then reloaded into the index register and the interrupting slot card is reset (lines F864 thorugh F86C). The routine then enables maskable interrupts and returns from the interrupt. It should be noted that each slot has 3 addresses. One for verifying an interrupt, one for reading the plug-in card command and one for resetting the card. These addresses can be found in the system memory map.

Time Delay Subroutine:

F870: - F87D: This subroutine is called by the Nonmaskable Interrupt routine and is used to mark time when waiting for shutters to settle after an emergency close-all-shutters command is sent. The delay is accomplished by a double counting looo. Initially both accumulators are cleared, and a count loop with accumulator A is begun (MINORLOOP). Accumulator A is incremented in this loop until its count reaches $FF (255) and then execution continues at MAJORLOOP. This loop increments accumulator B by one and then starts the MINORLOOP again. This sequence continues until accumulator B reaches ten at which time the delay subroutine ends. Counting the cycle times for each instruction in this subroutine and the number of times that the loop is executed results in a delay of 20,489 cycles or so. With a 3.58-MHz crystal operating the system (the cycle time being one over this frequency divided by four), this gives a delay of about 23 milliseconds. This is adequate for shutter settling before testing the shutter state.

IRQ Action Subroutine:

F87E - F8FA: This subroutine is called by the Interrupt Request routine and affects change in the shutters/interlocks according to the command byte read from the interrupting plug-in card. This subroutine can open or close any individual shutter or interlock as well as open or close all shutters or interlocks. This subroutine can also reset the system when interpreting the proper command. This subroutine begins at line F87E by loading the beginning address of the Action Table into the index register and storing it in locations $0010:$0011. The offset to this address is actually the command byte sent by the plug-in card, and this is added to the indexed address in line F883. There is no testing at this point to determine if the offset address is valid but this will be done later. The first set of potential actions to be taken by this subroutine occurs in lines F887 through F899. These lines comprise a set of compares and branch-on-equals to determine if the command sent is to either open or close all shutters, open or close all interlocks or to reset the system. If the command sent is not one of these special case operations, then the command byte is tested to determine if it is any other valid command (lines F89B through F8A1). It will be valid if it is between $04 and $23 (Hex) inclusively, if not then the subroutine is terminated.

Once a valid command is detected, it is tested to determine if it is a shutter-service command or an interlock-service command. Greater than or equal to $14 indicates an interlock service and less than $14 a shutter service. Once this is determined the least significant bit of the command is tested to determine if the command is a close command or an open command (either shutter or interlock). A logic 0 is a close command and a logic 1 is an open command. This test, along with the previous tests determines the exact nature of the command and the appropriate action can be taken.

The two service routines within this subroutine are called INTSERV and SHUTSERV. Within these two service routines are open and close routines called OPENINT, CLOSEINT (for the interlocks), OPENSHUT and CLOSESHUT (for the shutters). These routines perform the actual shutter and interlock operations as well as updating temporary storage locations for shutter and

interlock status and updating the shutter state indicator LED's. Updating an actual interlock or shuuter is done by fetching the appropriate mask word from the Action Table location addressed by the plug-in card command and either logical ANDing or ORing it with the current state of the shutters or interlocks. This method ensures that only the individual shutter or interlock in question is affected. After the correct action is taken and all status lights and/or status storage locations have been updated, the subroutine retuns to the Interrupt Request routine.

7.0 SYSTEM MEMORY MAPS
(Tables 5 through 8)

TABLE 5 - Interrupt Request Action Map

	Interrupt Card Data	HEX	Shutter Controller Action to Take	Loc. In EPROM	Data Out in Binary	HEX
0	0000 0000	00	Branch to Reset	0500	N/A	N/A
1	0000 0001	01	Unused	0501	N/A	N/A
2	0000 0010	02	Unused	0502	N/A	N/A
3	0000 0011	03	Unused	0503	N/A	N/A
4	0000 0100	04	Close Shutter #1	0504	1111 1110	FE
5	0000 0101	05	Open Shutter #1	0505	0000 0001	01
6	0000 0110	06	Close Shutter #2	0506	1111 1101	FD
7	0000 0111	07	Open Shutter #2	0507	0000 0010	02
8	0000 1000	08	Close Shutter #3	0508	1111 1011	FB
9	0000 1001	09	Open Shutter #3	0509	0000 0100	04
10	0000 1010	0A	CloseShutter #4	050A	1111 0111	F7
11	0000 1011	0B	Open Shutter #4	050B	0000 1000	08
12	0000 1100	0C	Close Shutter #5	050C	1110 1111	EF
13	0000 1101	0D	Open Shutter #5	050D	0001 0000	10
14	0000 1110	0E	Close Shutter #6	050E	1101 1111	DF
15	0000 1111	0F	Open Shutter #6	050F	0010 0000	20
16	0001 0000	10	Close Shutter #7	0510	1011 1111	BF
17	0001 0001	11	Open Shutter #7	0511	0100 0000	40
18	0001 0010	12	Close Shutter #8	0512	0111 1111	7F
19	0001 0011	13	Open Shutter #8	0513	1000 0000	80
20	0001 0100	14	Close Interlock #1	0514	0000 0001	01
21	0001 0101	15	Open Interlock #1	0515	1111 1110	FE
22	0001 0110	16	Close Interlock#2	0516	0000 0010	02
23	0001 0111	17	Open Interlock #2	0517	1111 1101	FD
24	0001 1000	18	Close Interlock#3	0518	0000 0100	04
25	0001 1001	19	Open Interlock #3	0519	1111 1011	FB
26	0001 1010	1A	Close Interlock #4	051A	0000 1000	08
27	0001 1011	1B	Cpen Interlock #4	051B	1111 0111	F7
28	0001 1100	1C	Close Interlock #5	051C	0001 0000	10
29	0001 1101	1D	Open Interlock #5	051D	1110 1111	EF
30	0001 1110	1E	Close Interlock #6	051E	0010 0000	20
31	0001 1111	1F	Open Interlock #6	051F	1101 1111	DF
32	0010 0000	20	Close Interlock #7	0520	0100 0000	40
33	0010 0001	21	Open Interlock #7	0521	1011 1111	BF
34	0010 0010	22	Close Interlock #8	0522	1000 0000	80
35	0010 0011	23	Open Interlock #8	0523	0111 1111	7F
36	0010 0100	24	Close All Shutters	0524	N/A	N/A
37	0010 0101	25	Open All Shutters	0525	N/A	N/A
38	0010 0110	26	Close All Interlocks	0526	N/A	N/A
39	0010 0111	27	Open All Interlocks	0527	N/A	N/A

TABLE 6 - System Memory Map

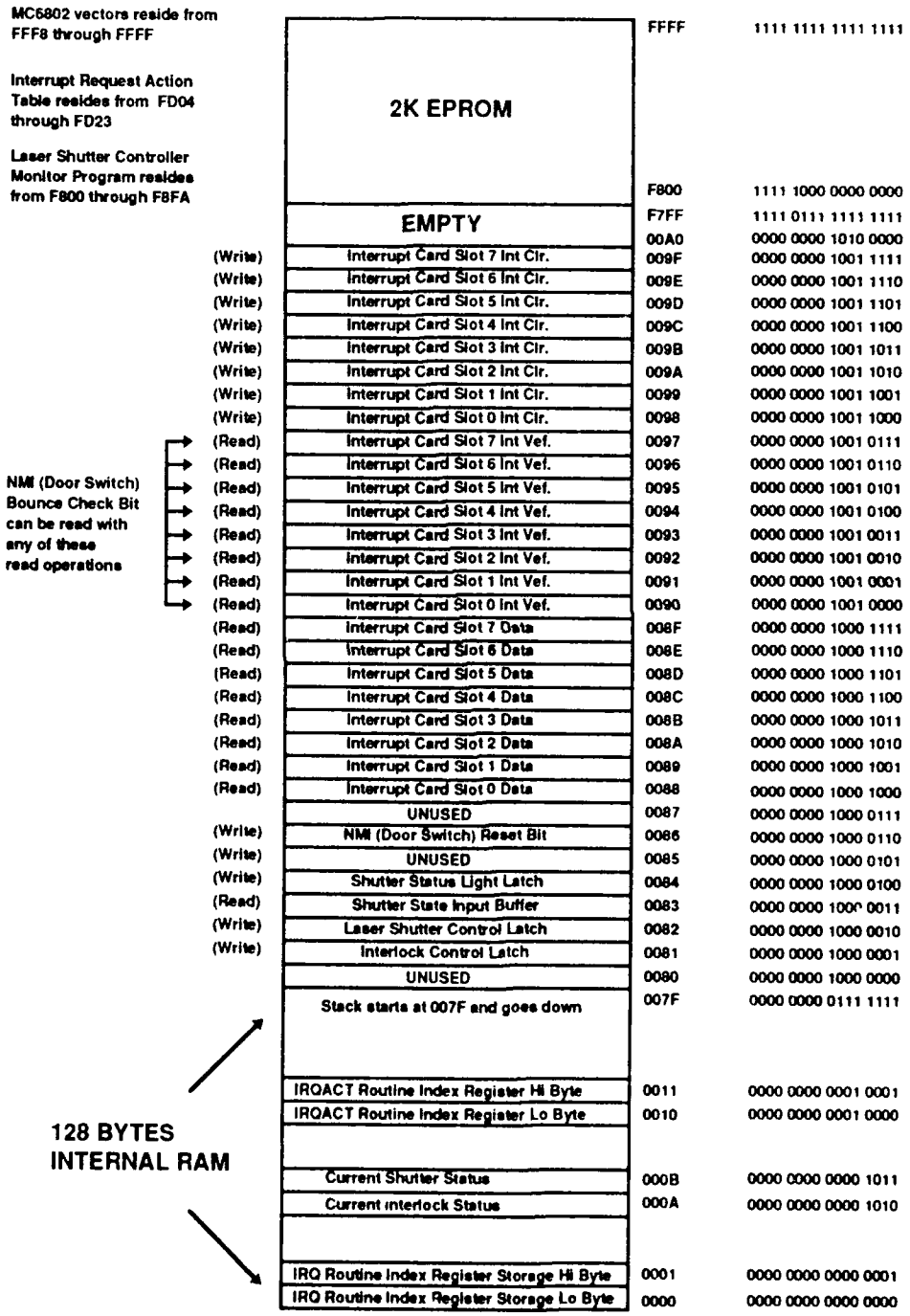


TABLE 7 - PROM A Memory Map

Address HEX	A4	A3	A2	A1	A0	Description	Data D7	D6	D5	D4	D3	D2	D1	D0	HEX
00	0	0	0	0	0		1	1	1	1	1	1	1	1	FF
01	0	0	0	0	1	Interlock Latch	1	1	0	1	1	1	1	1	DF
02	0	0	0	1	0	Laser Shutter Latch	1	1	1	0	1	1	1	1	EF
03	0	0	0	1	1	Shutter State Input Buf.	1	1	1	1	0	1	1	1	F7
04	0	0	1	0	0	Shut. State Lgt. Latch	1	1	1	1	1	0	1	1	FB
05	0	0	1	0	1	Unused	1	1	1	1	1	1	1	1	FF
06	0	0	1	1	0	Door Switch Reset Bit	1	1	1	1	1	1	1	0	FE
07	0	0	1	1	1		1	1	1	1	1	1	1	1	FF
08	0	1	0	0	0		1	1	1	1	1	1	1	1	FF
09	0	1	0	0	1		1	1	1	1	1	1	1	1	FF
0A	0	1	0	1	0		1	1	1	1	1	1	1	1	FF
0B	0	1	0	1	1		1	1	1	1	1	1	1	1	FF
0C	0	1	1	0	0		1	1	1	1	1	1	1	1	FF
0D	0	1	1	0	1		1	1	1	1	1	1	1	1	FF
0E	0	1	1	1	0		1	1	1	1	1	1	1	1	FF
0F	0	1	1	1	1		1	1	1	1	1	1	1	1	FF
10	1	0	0	0	0		1	1	1	1	1	1	1	1	FF
11	1	0	0	0	1		1	1	1	1	1	1	1	1	FF
12	1	0	0	1	0		1	1	1	1	1	1	1	1	FF
13	1	0	0	1	1		1	1	1	1	1	1	1	1	FF
14	1	0	1	0	0		1	1	1	1	1	1	1	1	FF
15	1	0	1	0	1		1	1	1	1	1	1	1	1	FF
16	1	0	1	1	0		1	1	1	1	1	1	1	1	FF
17	1	0	1	1	1		1	1	1	1	1	1	1	1	FF
18	1	1	0	0	0	Interrupt Clr. Slot 0	1	1	1	1	1	1	0	1	FD
19	1	1	0	0	1	Interrupt Clr. Slot 1	1	1	1	1	1	1	0	1	FD
1A	1	1	0	1	0	Interrupt Clr. Slot 2	1	1	1	1	1	1	0	1	FD
1B	1	1	0	1	1	Interrupt Clr. Slot 3	1	1	1	1	1	1	0	1	FD
1C	1	1	1	0	0	Interrupt Clr. Slot 4	1	1	1	1	1	1	0	1	FD
1D	1	1	1	0	1	Interrupt Clr. Slot 5	1	1	1	1	1	1	0	1	FD
1E	1	1	1	1	0	Interrupt Clr. Slot 6	1	1	1	1	1	1	0	1	FD
1F	1	1	1	1	1	Interrupt Clr. Slot 7	1	1	1	1	1	1	0	1	FD

Laser Shutter Controller
Address Decoder Prom A

TABLE 8 - PROM B Memory Map

Address							Data								
HEX	A4	A3	A2	A1	A0	Description	D7	D6	D5	D4	D3	D2	D1	D0	HEX
00	0	0	0	0	0		1	1	1	1	1	1	1	1	FF
01	0	0	0	0	1		1	1	1	1	1	1	1	1	FF
02	0	0	0	1	0		1	1	1	1	1	1	1	1	FF
03	0	0	0	1	1		1	1	1	1	1	1	1	1	FF
04	0	0	1	0	0		1	1	1	1	1	1	1	1	FF
05	0	0	1	0	1		1	1	1	1	1	1	1	1	FF
06	0	0	1	1	0		1	1	1	1	1	1	1	1	FF
07	0	0	1	1	1		1	1	1	1	1	1	1	1	FF
08	0	1	0	0	0	Slot 0 Data	1	1	1	1	1	1	1	0	FE
09	0	1	0	0	1	Slot 1 Data	1	1	1	1	1	1	0	1	FD
0A	0	1	0	1	0	Slot 2 Data	1	1	1	1	1	0	1	1	FB
0B	0	1	0	1	1	Slot 3 Data	1	1	1	1	0	1	1	1	F7
0C	0	1	1	0	0	Slot 4 Data	1	1	1	0	1	1	1	1	EF
0D	0	1	1	0	1	Slot 5 Data	1	1	0	1	1	1	1	1	DF
0E	0	1	1	1	0	Slot 6 Data	1	0	1	1	1	1	1	1	BF
0F	0	1	1	1	1	Slot 7 Data	0	1	1	1	1	1	1	1	7F
10	1	0	0	0	0	Slot 0 Interrupt Verify	1	1	1	1	1	1	1	0	FE
11	1	0	0	0	1	Slot 1 Interrupt Verify	1	1	1	1	1	1	0	1	FD
12	1	0	0	1	0	Slot 2 Interrupt Verify	1	1	1	1	1	0	1	1	FB
13	1	0	0	1	1	Slot 3 Interrupt Verify	1	1	1	1	0	1	1	1	F7
14	1	0	1	0	0	Slot 4 Interrupt Verify	1	1	1	0	1	1	1	1	EF
15	1	0	1	0	1	Slot 5 Interrupt Verify	1	1	0	1	1	1	1	1	DF
16	1	0	1	1	0	Slot 6 Interrupt Verify	1	0	1	1	1	1	1	1	BF
17	1	0	1	1	1	Slot 7 Interrupt Verify	0	1	1	1	1	1	1	1	7F
18	1	1	0	0	0	Interrupt Clr. Slot 0	1	1	1	1	1	1	1	0	FE
19	1	1	0	0	1	Interrupt Clr. Slot 1	1	1	1	1	1	1	0	1	FD
1A	1	1	0	1	0	Interrupt Clr. Slot 2	1	1	1	1	1	0	1	1	FB
1B	1	1	0	1	1	Interrupt Clr. Slot 3	1	1	1	1	0	1	1	1	F7
1C	1	1	1	0	0	Interrupt Clr. Slot 4	1	1	1	0	1	1	1	1	EF
1D	1	1	1	0	1	Interrupt Clr. Slot 5	1	1	0	1	1	1	1	1	DF
1E	1	1	1	1	0	Interrupt Clr. Slot 6	1	0	1	1	1	1	1	1	BF
1F	1	1	1	1	1	Interrupt Clr. Slot 7	0	1	1	1	1	1	1	1	7F

Laser Shutter Controller
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